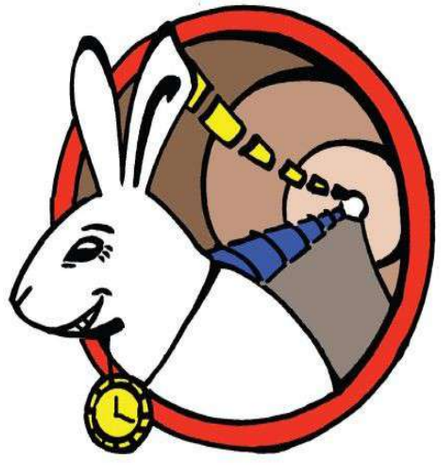


The IDROGEN board, an enhance WhiteRabbit node

Antoine Back, Olivier Bourrion, Chafik Cheikali, **Daniel Charlet**, Eric Plaige, Paul-Eric Pottie, Monique Taurigna, Cédric Viou

T+REFIMEVE June 2023

Outline

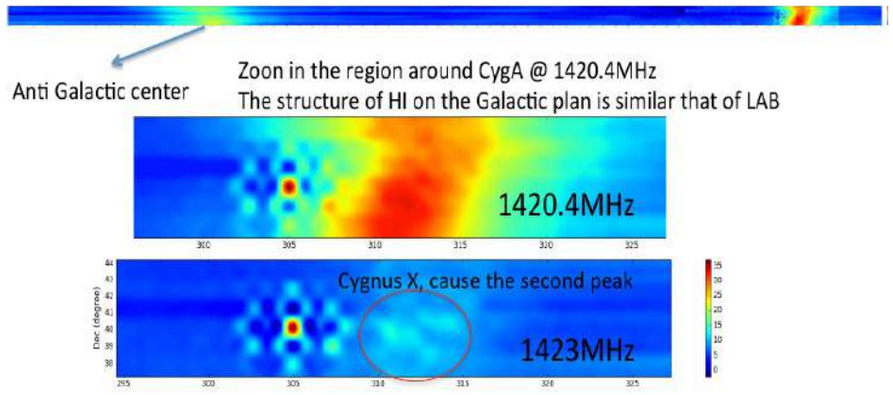
- WR motivations
- White Rabbit overview
- IDROGEN system
  - Hardware_Firmware_Software

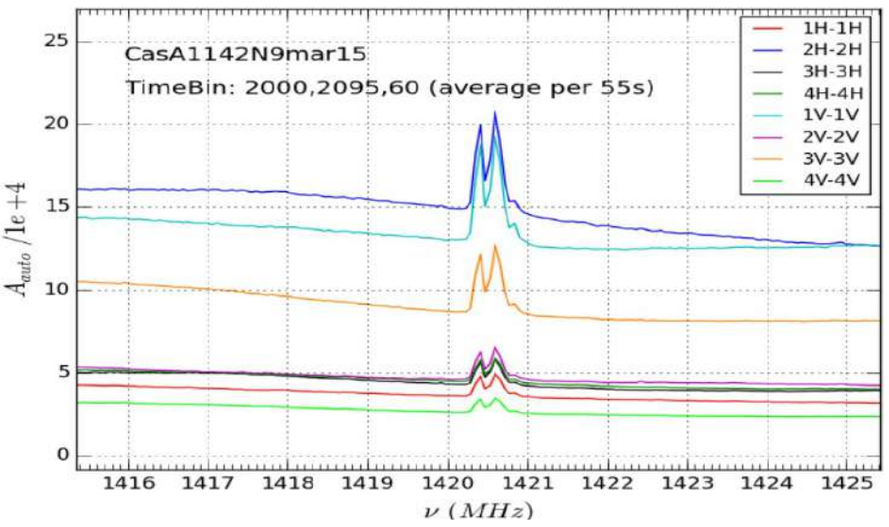
WR Motivations

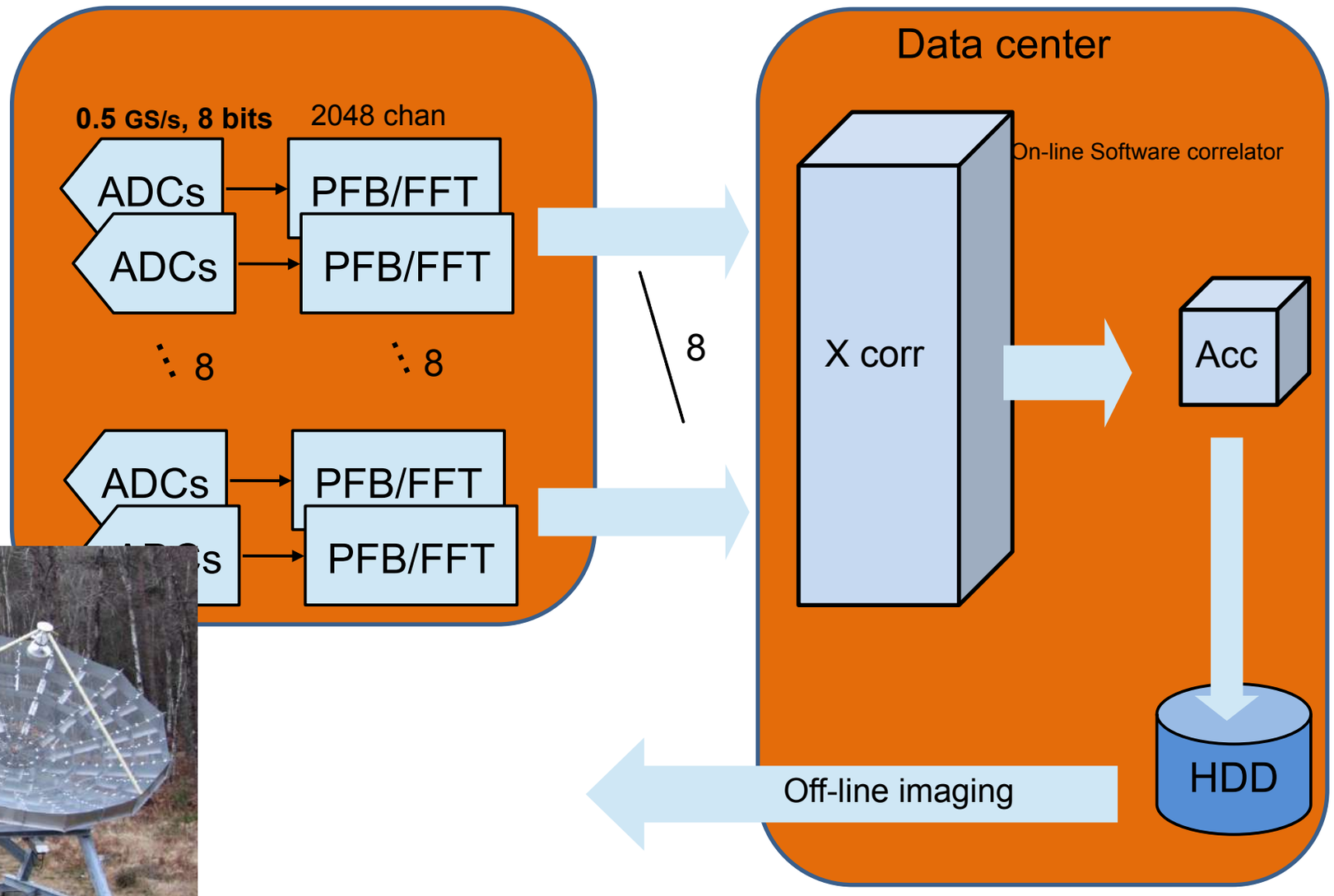
- Radio astronomie : multi-dish synchronisation and events time tagging
- Physics detector :
  - multi-detector synchronisation
  - time tagging for trigger less system
- Accelerator synchronisation
- Master oscillator distribution

WR motivations : Radio astronomy PAON IV

Radio telescope demonstrator for mapping in 3D of the atomic hydrogen in the universe

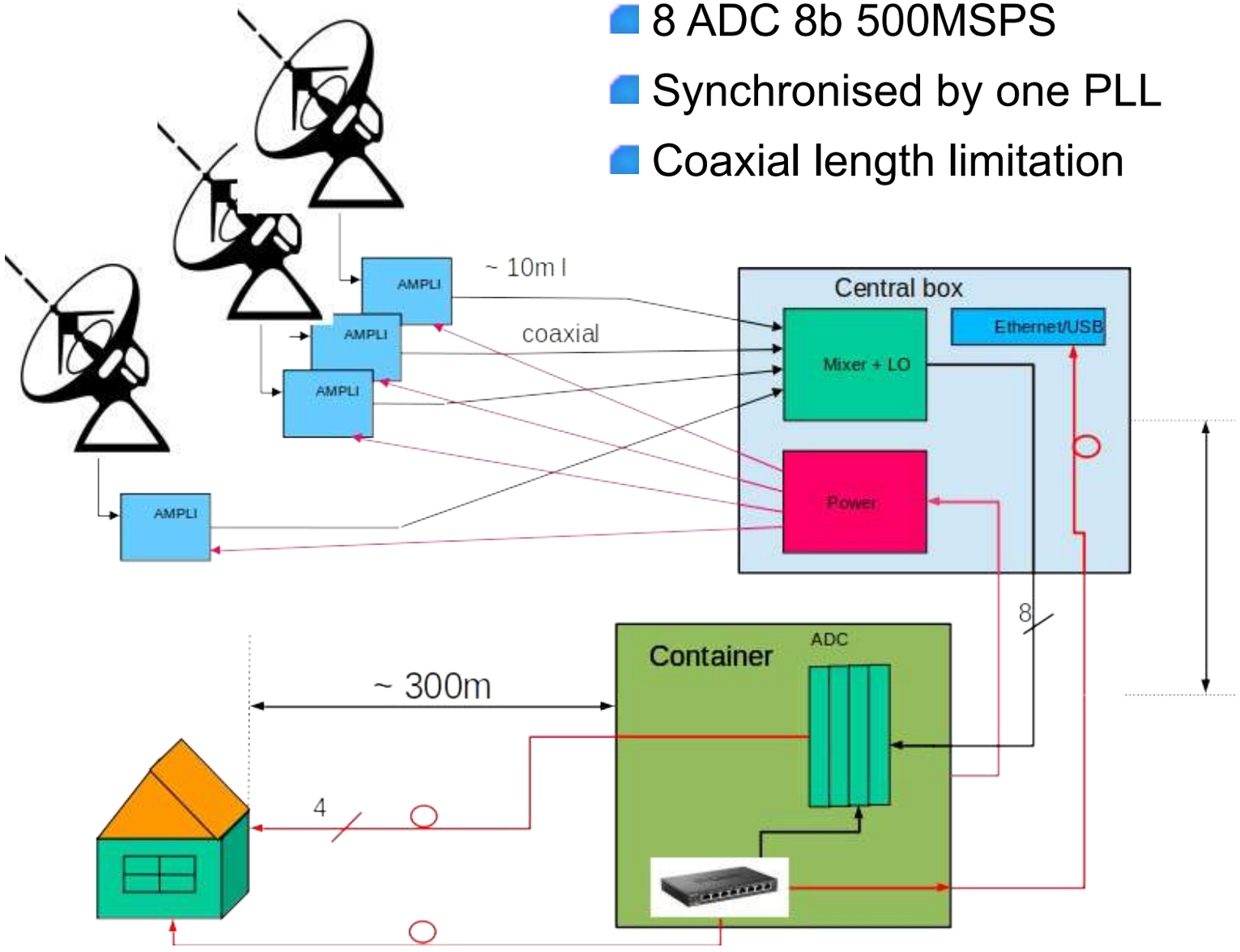




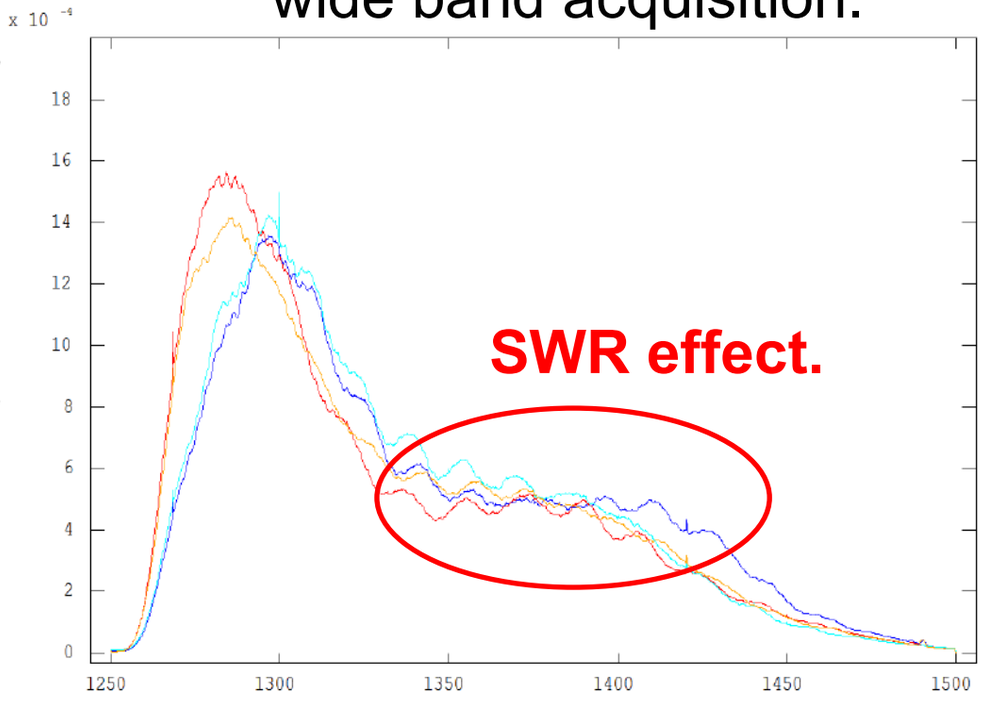


PAON IV : previous architecture

- Interferometer 4 radio dishes of 5m
  - Centralized coding architecture
  - High bandwidth : 250MHz
  - 8 ADC 8b 500MSPS
  - Synchronised by one PLL
  - Coaxial length limitation



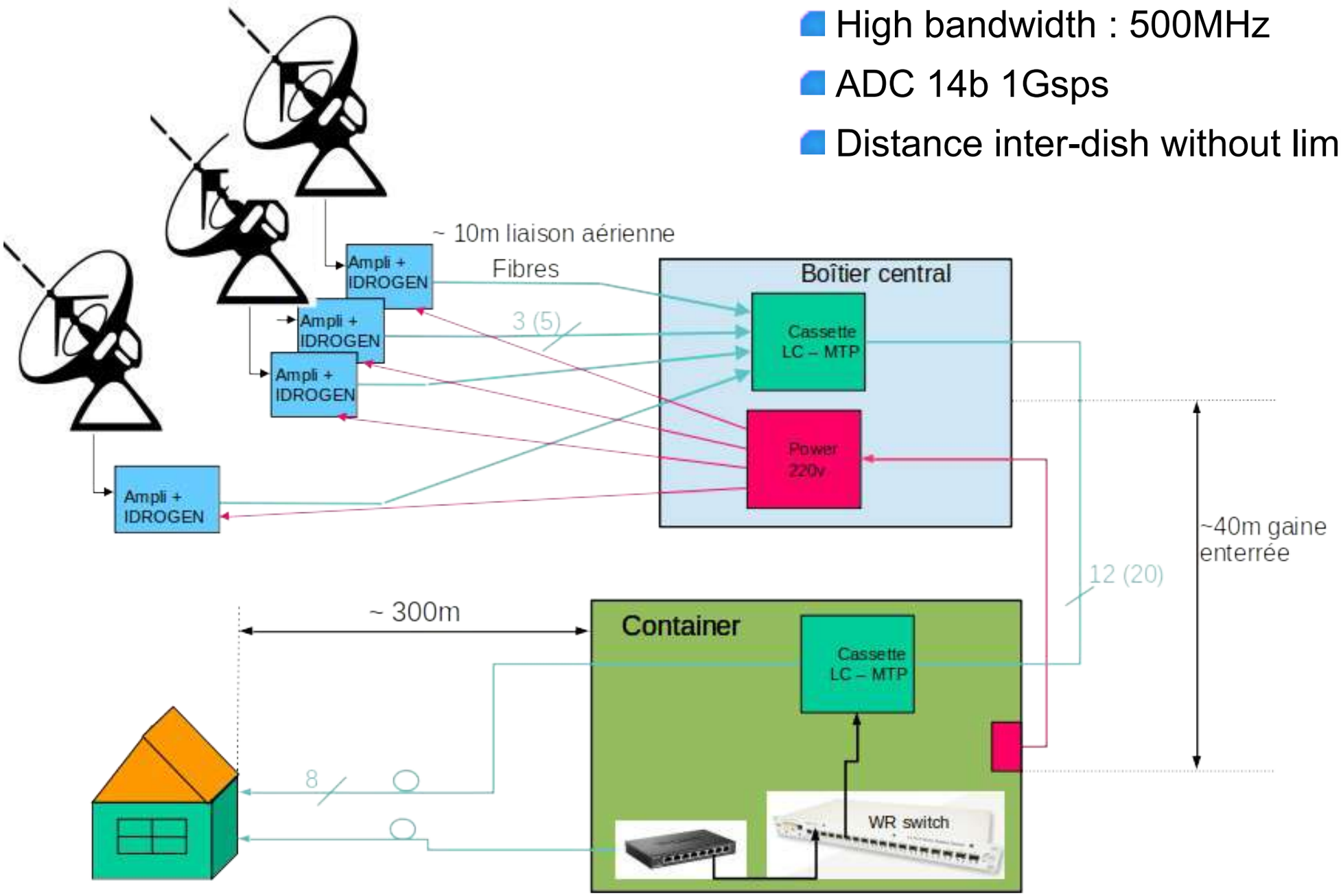
SWR depends of:
RF cable length,
Adaptation mismatch,
wide band acquisition.



Systèmes de Référence Temps-Espace

PAON IV : new architecture

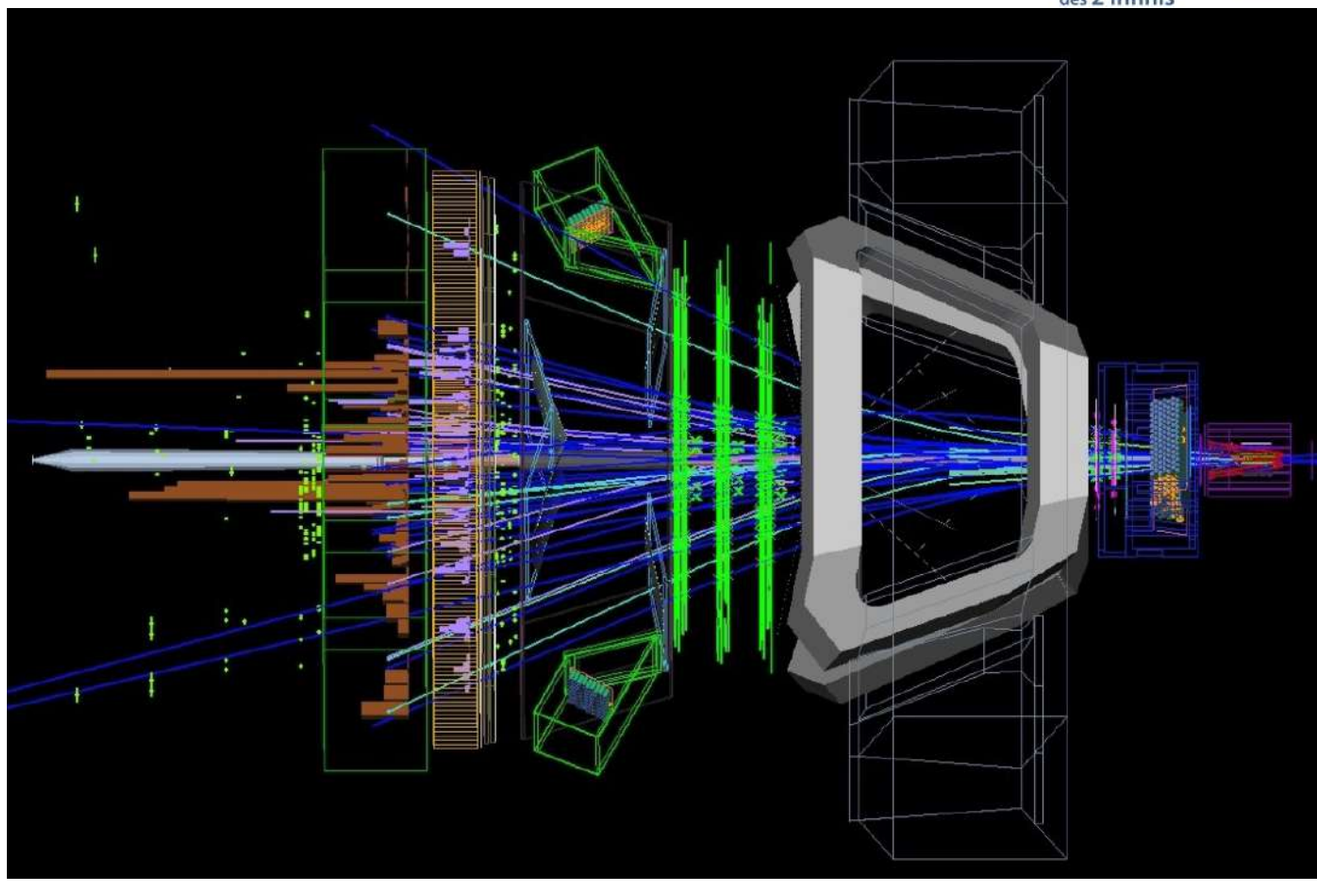
- Interferometer 4 radio dishes of 5m
  - Synchronised by the WhiteRabbit
  - High bandwidth : 500MHz
  - ADC 14b 1Gsps
  - Distance inter-dish without limitation

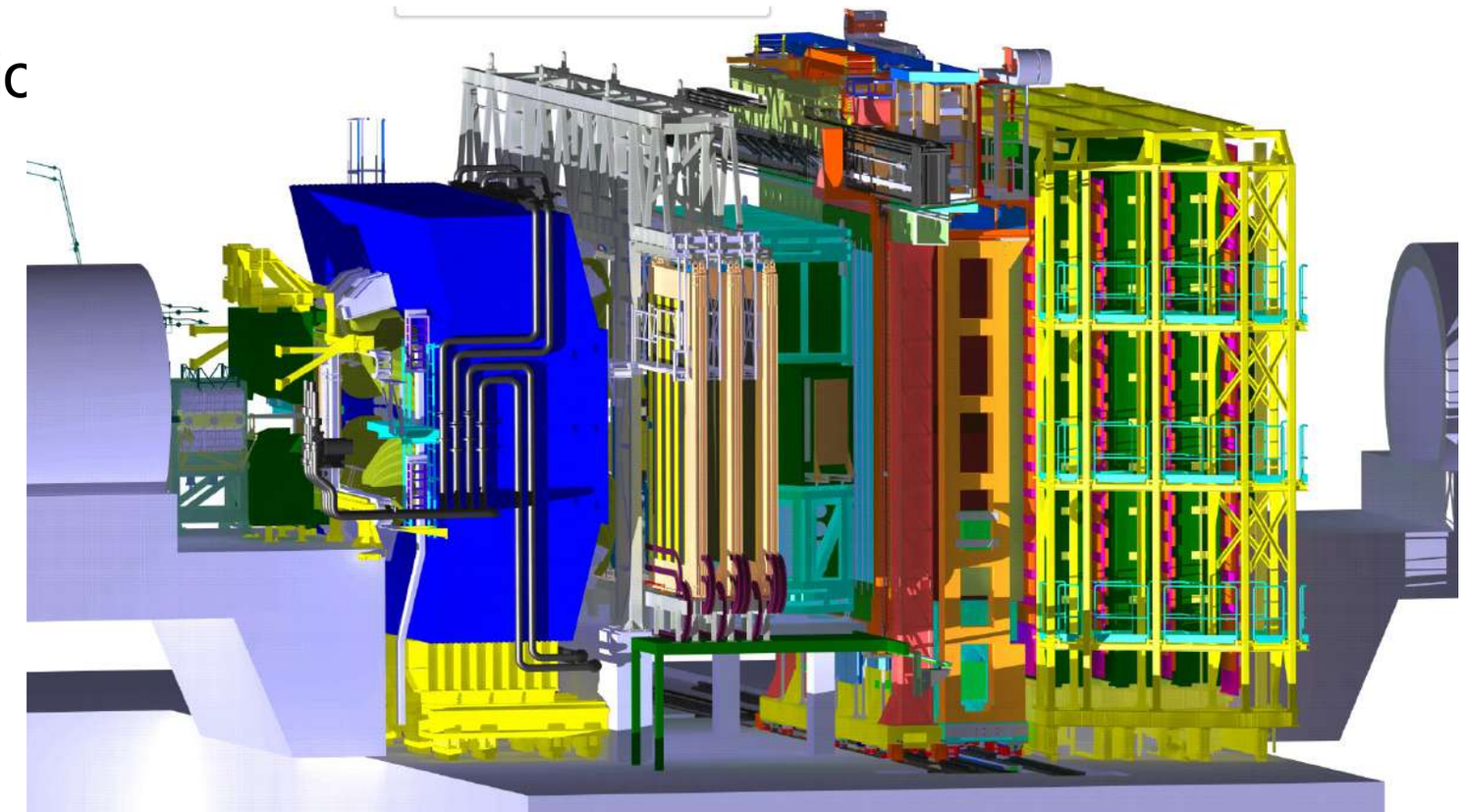


Systèmes de Référence Temps-Espace

WR Motivations : Multi-detectors LHCb

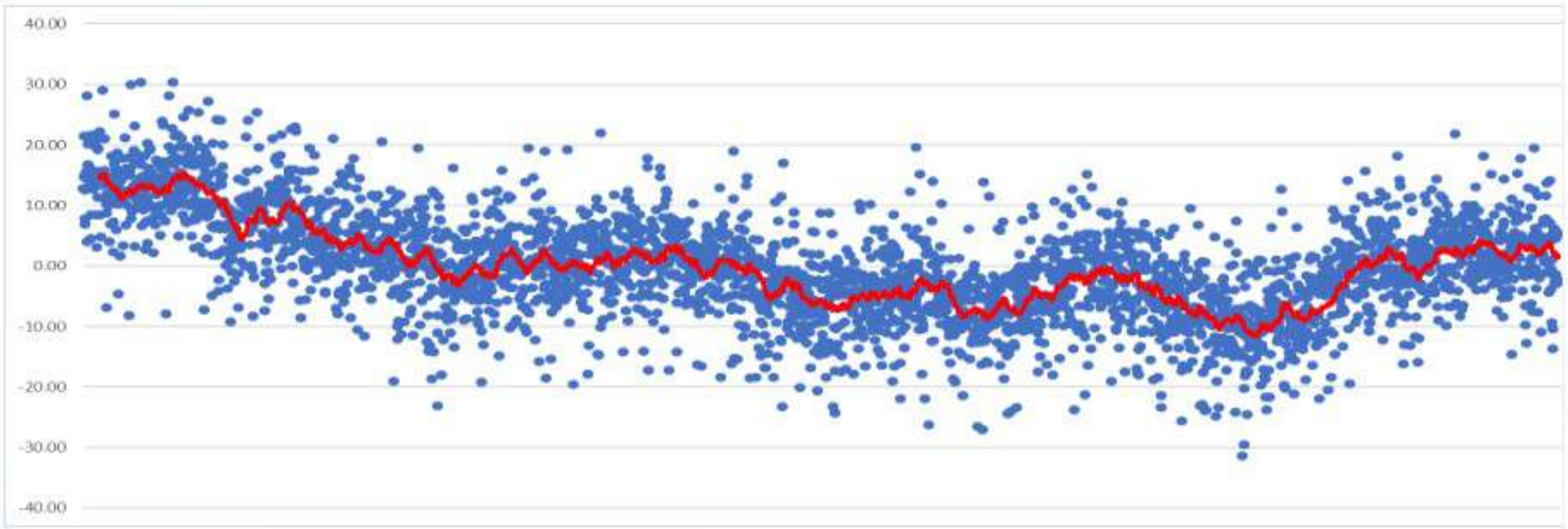
- LHCb detector
- 7 sub-detectors
- 20m x 20m
- Further million of acquisitions chanels
- All systems must be synchronize with the same clock (40MHz)
- A complex and long calibration time is mandatory
- Clock drift during physic aquistic

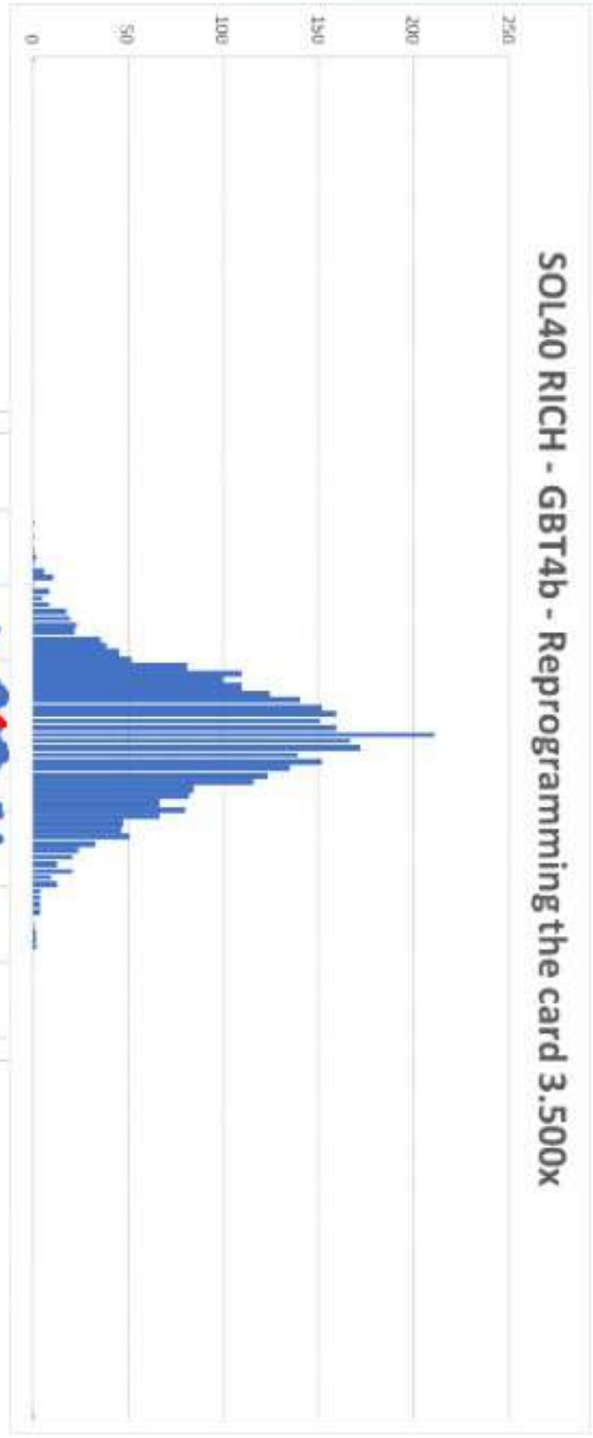




Clock drift over time

SOL40 RICH – GBT4b – Reprogramming SOL40 3500x
Over 5 days of test
Center of recovered clock distribution drifted over ~25ps
Most likely due to temperature

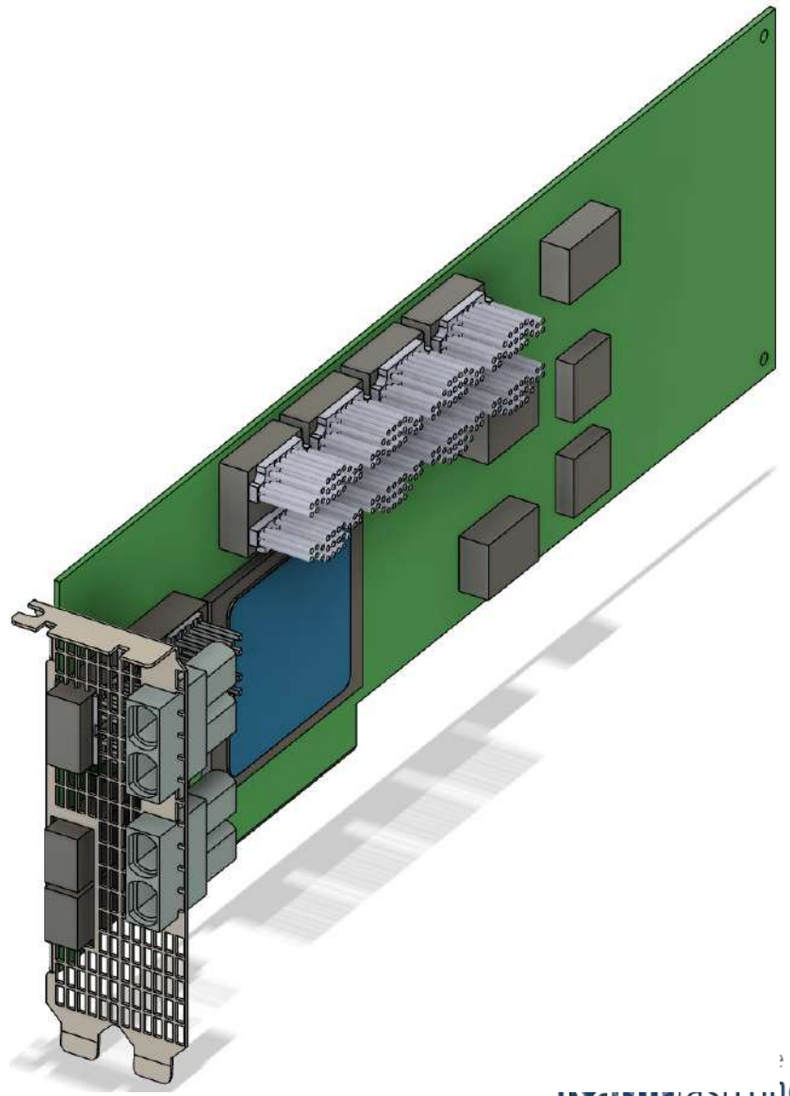




The resolution of the SOL40 PLL shift is ~100ps

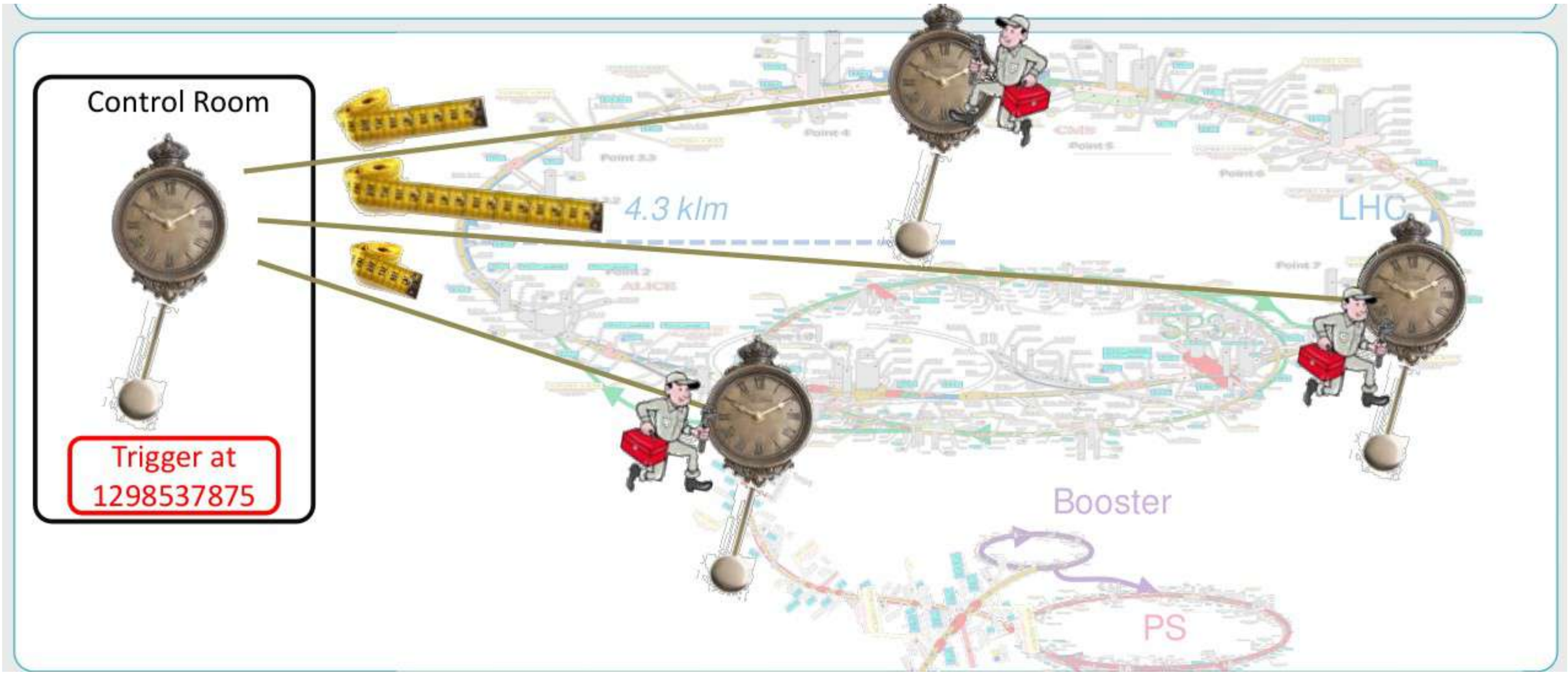
WR Motivations : Multi-detectors PCIE400

- Data acquisition and event formatting board for the futur LHC upgrade
- More than to 500 boards for a detector
- WhiteRabbit clock distribution (5ps)
- Foreseen characteristics
  - Agilex7 M-series AGMF039R47A1E2V
  - No DDR memory
  - Use of PC RAM or HBM2e instead
  - Up to 48x26Gbps NRZ for FE
  - PCIe Gen 5 / CXL or 400GbE
  - Low jitter PLL < 100 fs RMS
  - White Rabbit clock distribution (1ps) (SFP+)



Accelerator : Master oscillator distribution

- Real-timed communication system : tight time constraints
- Long distances between nodes : long transmission delays
- Numbers of nodes : several hundred
- Dynamic changes to the numbers of nodes : not easy



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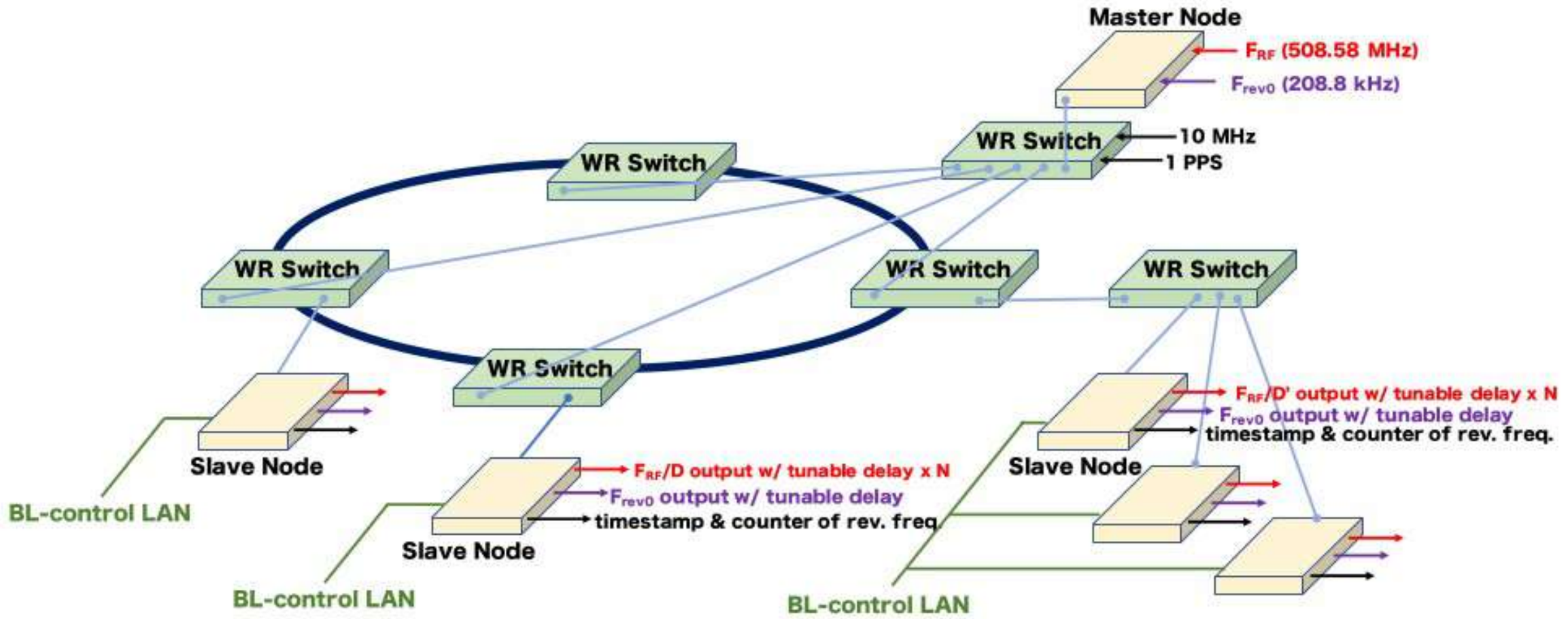
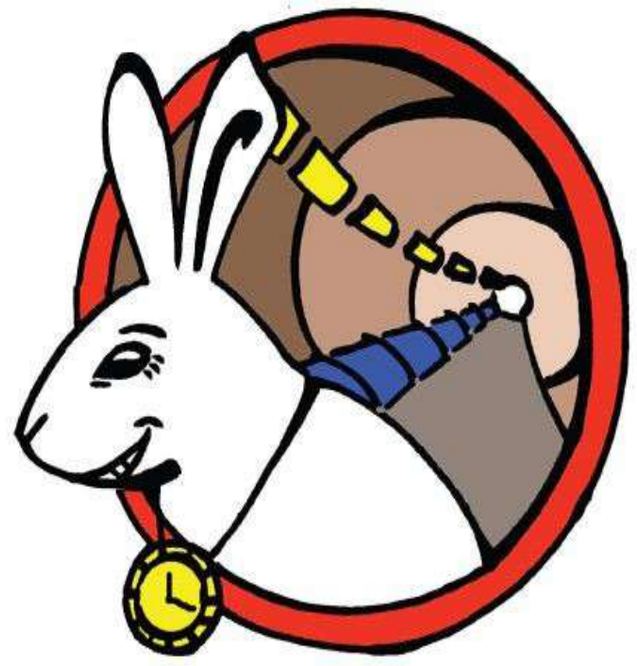
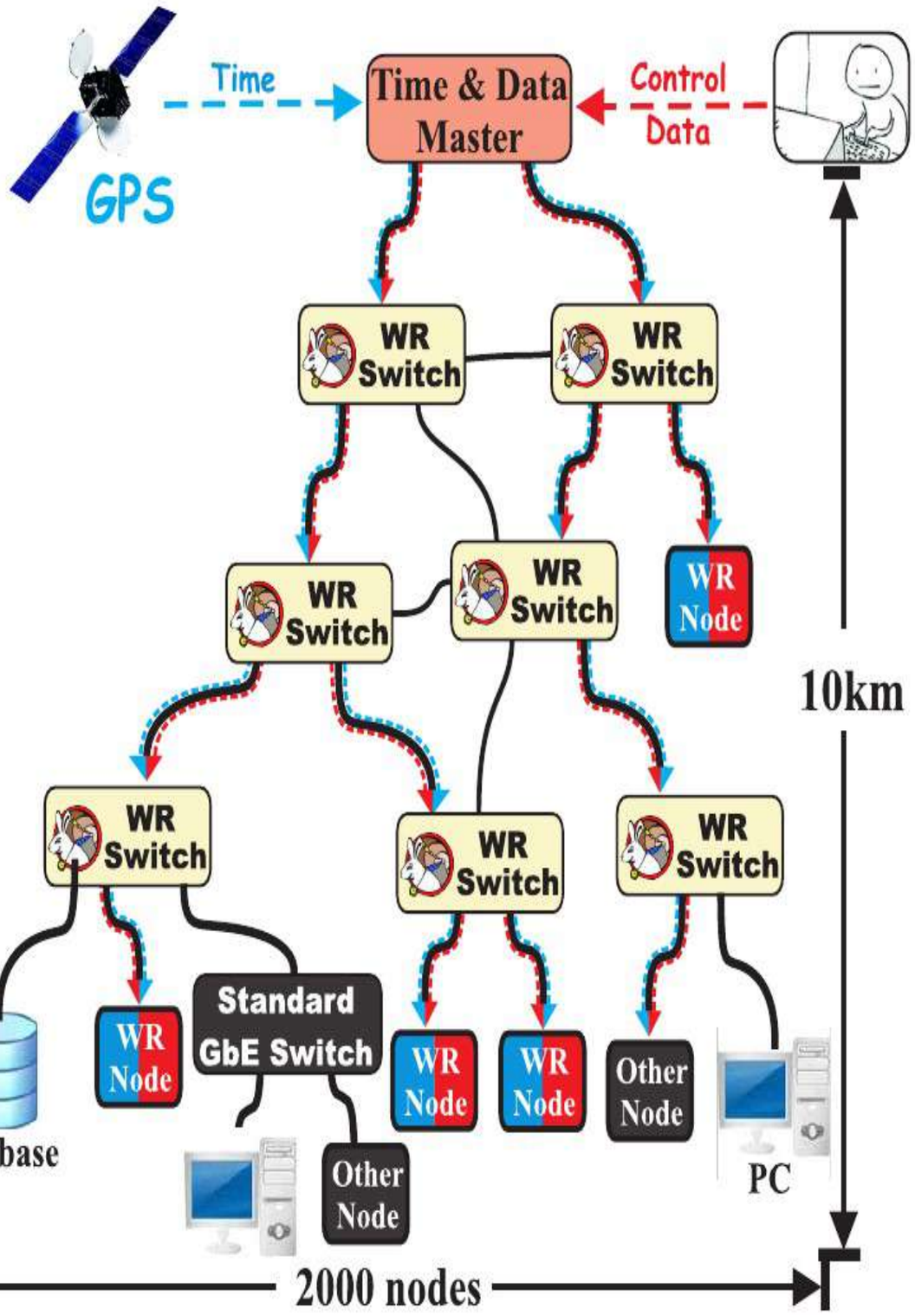


Systèmes de Référence Temps-Espace

WhiteRabbit

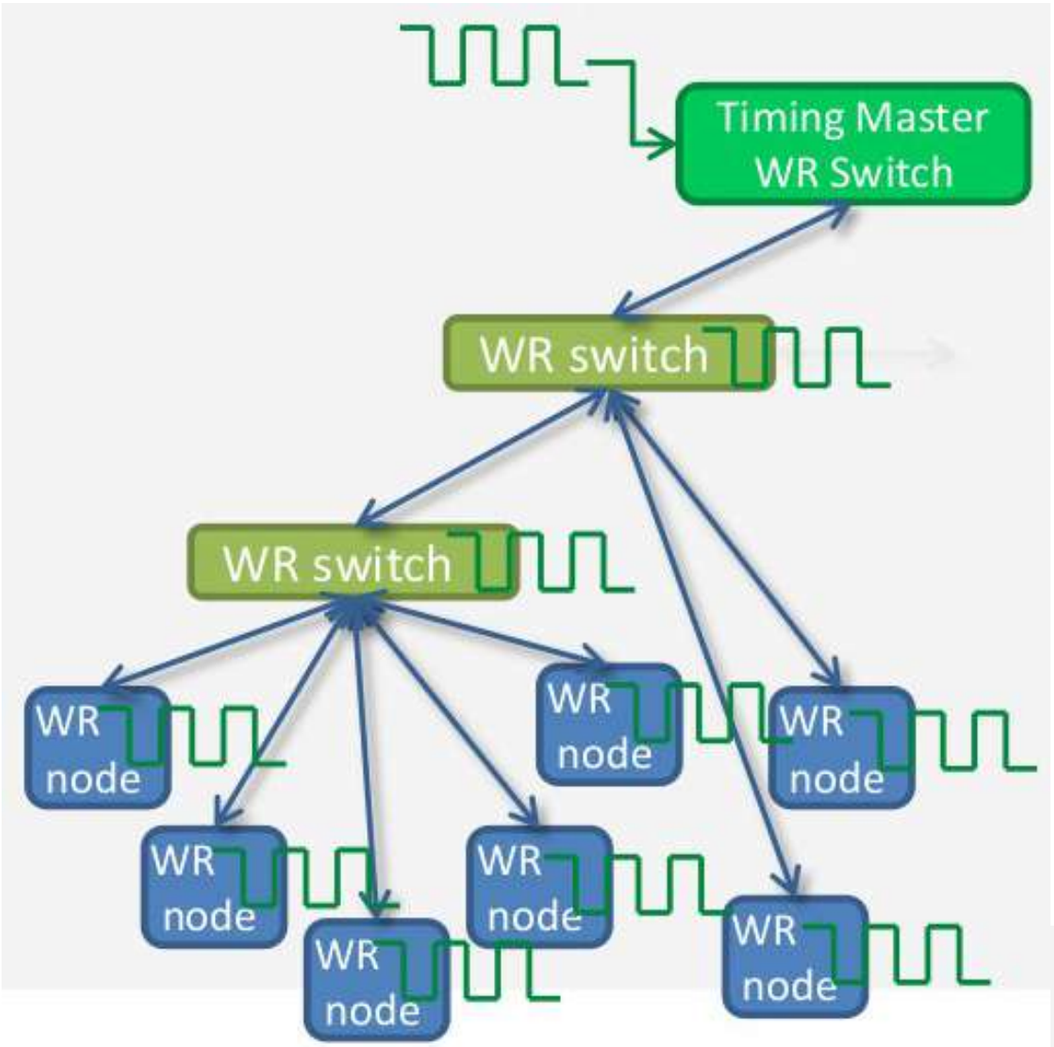


White Rabbit principle : Enhanced Ethernet

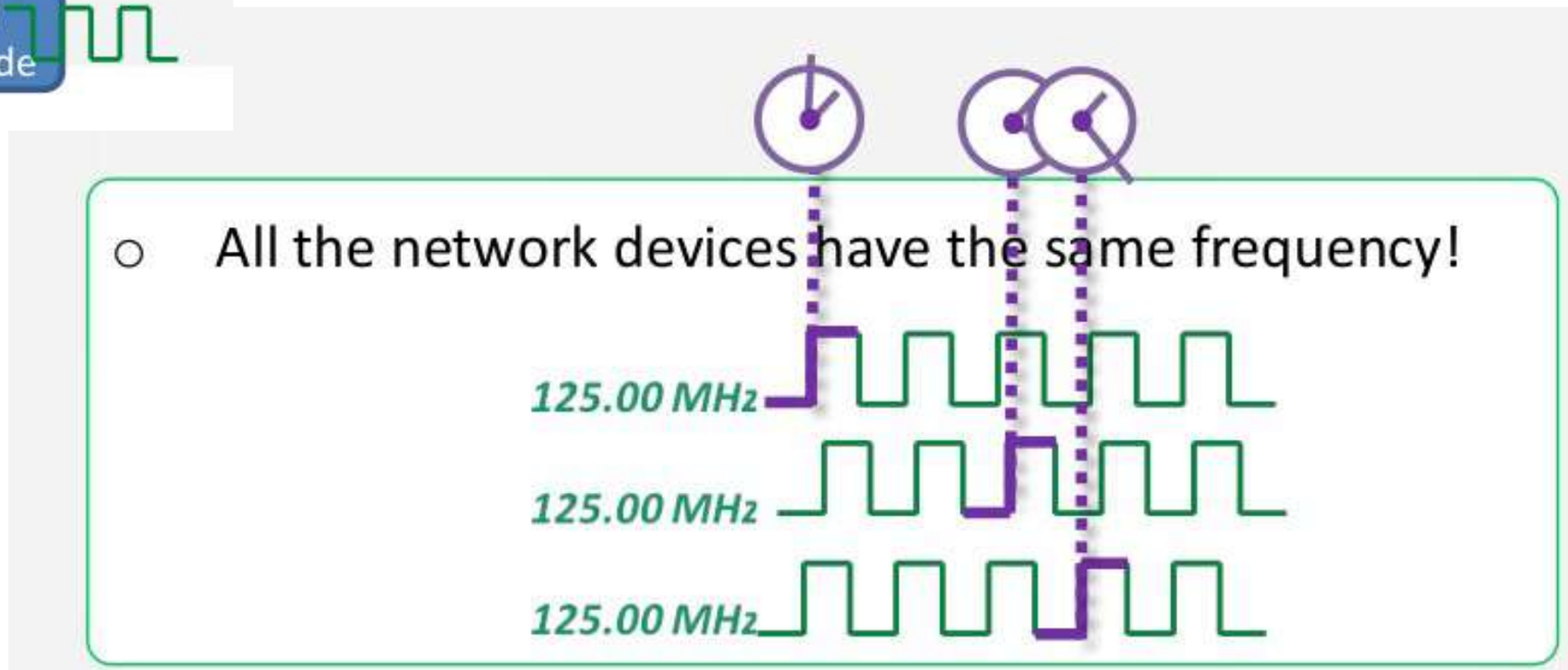


- An extension of Ethernet which provides :
  - Synchronous mode (Syn-E) – common clock for physical layer in entire network, allowing for precise time and frequency transfer
  - Deterministic routing latency – a guarantee that packet transmission delay between two stations will never exceed a certain boundary.
- Technology overview
  - Precision Time Protocole (IEEE1588)
  - Synchronous Ethernet
  - DDMTD Phase tracking (Digital Dual Mixer Domain) …

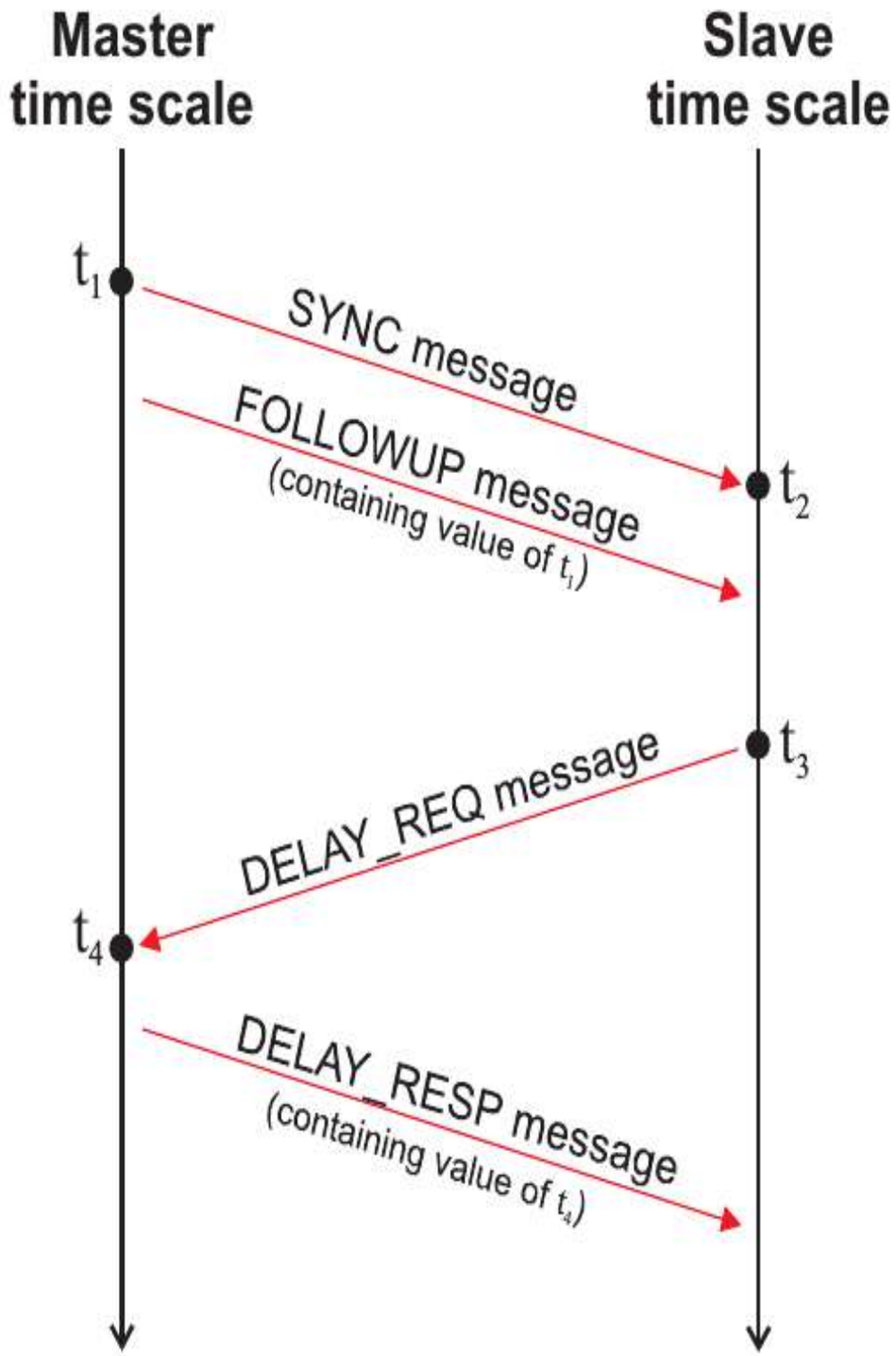
Synchronous Ethernet (Sync-E)



- All network nodes use the same physical layer clock,
- Clock is encode in the Ethernet carrier and recovered by the receiver chip(PHY)
- A master and unique clock for the whole network
- Synchronous digital hierarchy
- High precision clock definition, 20 better than standard Ethernet clock



Precision Time Protocol (IEEE1588)



- Packet-based synchronization protocol
- Synchronizes local clock with the master clock by measuring and compensating the delay introduced by the link.
- Link delay evaluated by measuring and exchanging packets tx/rx timestamps
- PTP is used only for compensation of the clock offset

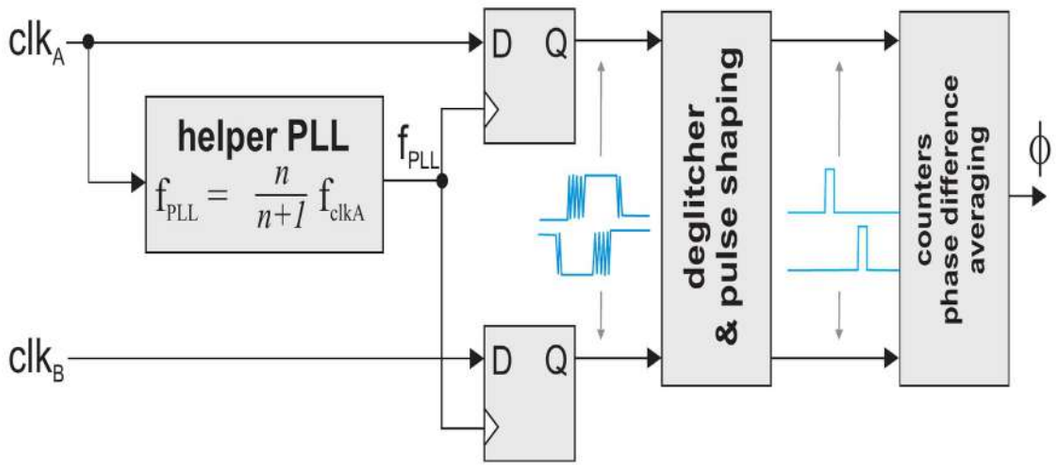
Having values of t1 ...t4 , slave can:

- calculate one-way link delay:

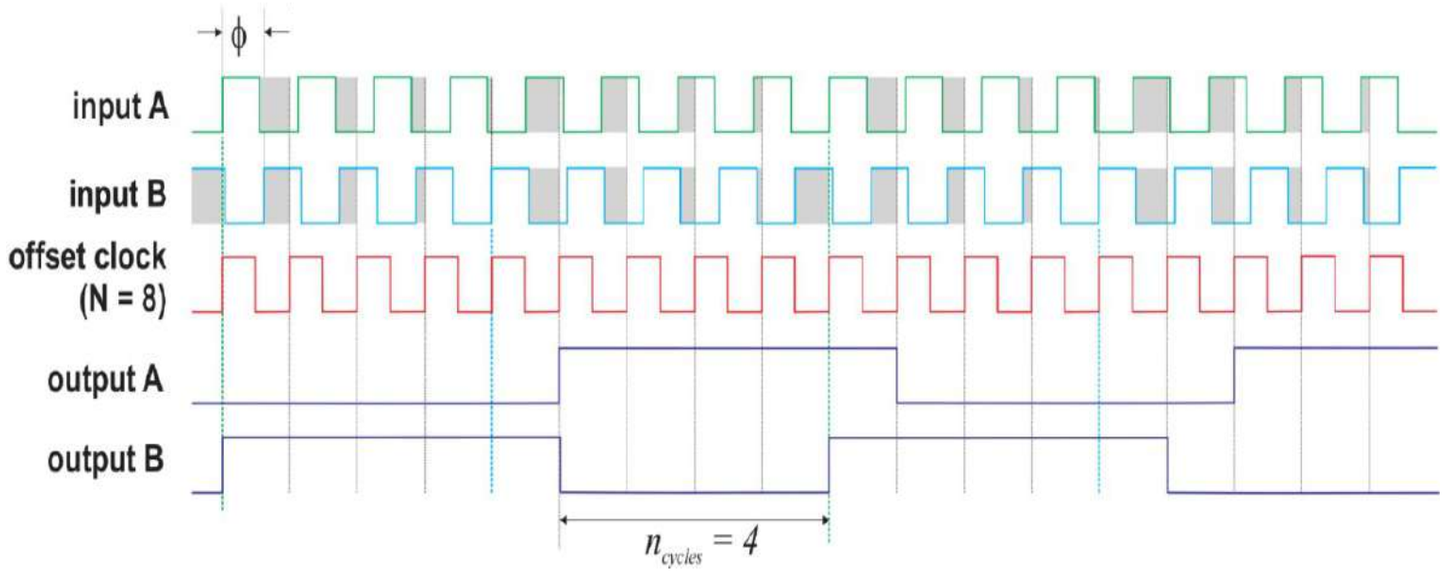
$$\delta ms = ((t4 - t1) - (t3 - t2))/2$$

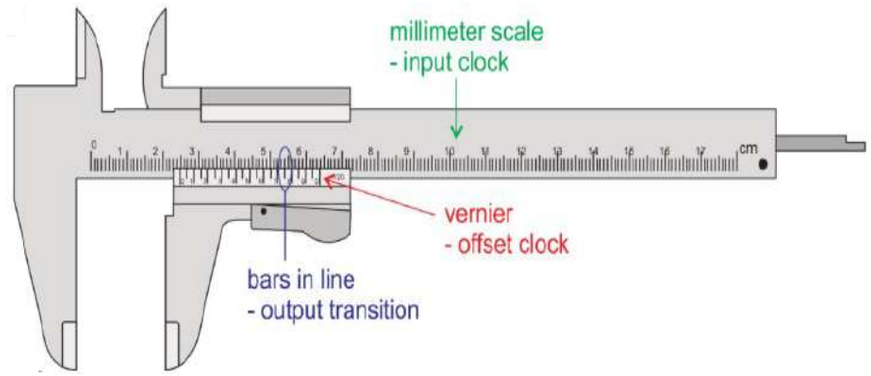
- syntonize its clock rate with the master by tracking the value of
  t2 − t1
- compute clock offset:
  offset = t2 − t1 + δms

Digital Dual Mixer Time Domaine phase detector (DDMTD)



- Measure the phase shift between transmit and receive clock on
- the master side, taking the advantage of Synchronous Ethernet.
- Monitor phase of bounced-back clock continuously.
- Phase-locked loop in the slave follows the phase changes measured by the master.

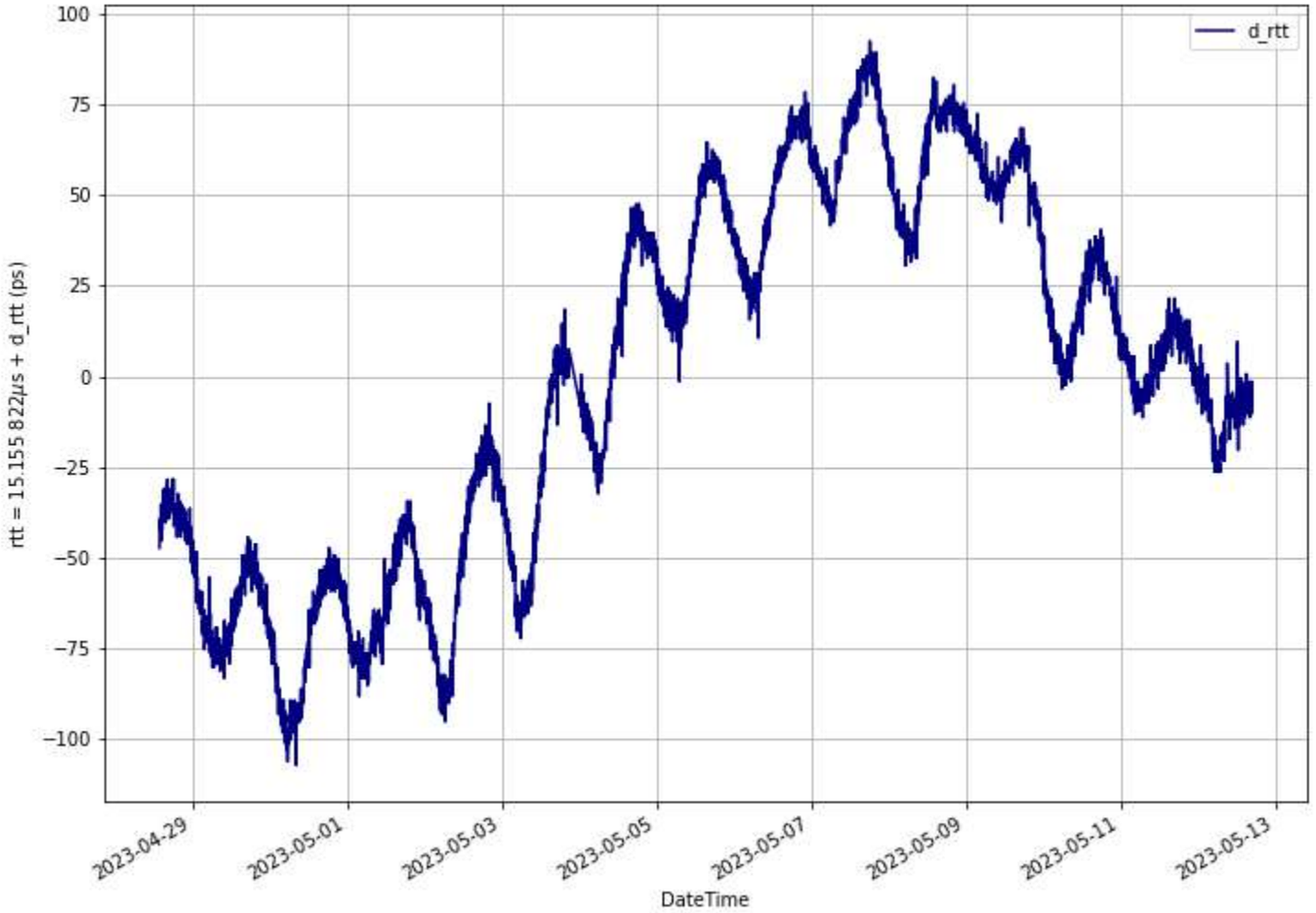




Systèmes de Référence Temps-Espace

WhiteRabbit supervision

```
WR PTP Core Sync Monitor v 1.0
Esc = exit

TAI Time:                   Thu, Jan 1, 1970, 00:03:48

wru1: Link up   (RX: 685, TX: 281), mode: WR Slave   Locked  Calibrated
IPv4: BOOTP running

PTP status: slave

Synchronization status:

Servo state:                TRACK_PHASE
Phase tracking:             ON
Synchronization source:
Aux clock status:

Timing parameters:

Round-trip time (mu):     691831 ps
Master-slave delay:       349132 ps
Master PHY delays:        TX: 46407 ps, RX: 168643 ps
Slave PHY delays:         TX: 46407 ps, RX: 175043 ps
Total link asymmetry:        -6433 ps
Cable rtt delay:          255331 ps
Clock offset:                  0 ps
Phase setpoint:              528 ps
Skew:                          5 ps
Manual phase adjustment:       0 ps
Update counter:              174
--
```



- WR debugging
  - Small operating system include in the WR core
  - Serial communication by USB or Ethernet
  - Status of the link : Delay, transceiver
  - Control of the link : PPS,configuration

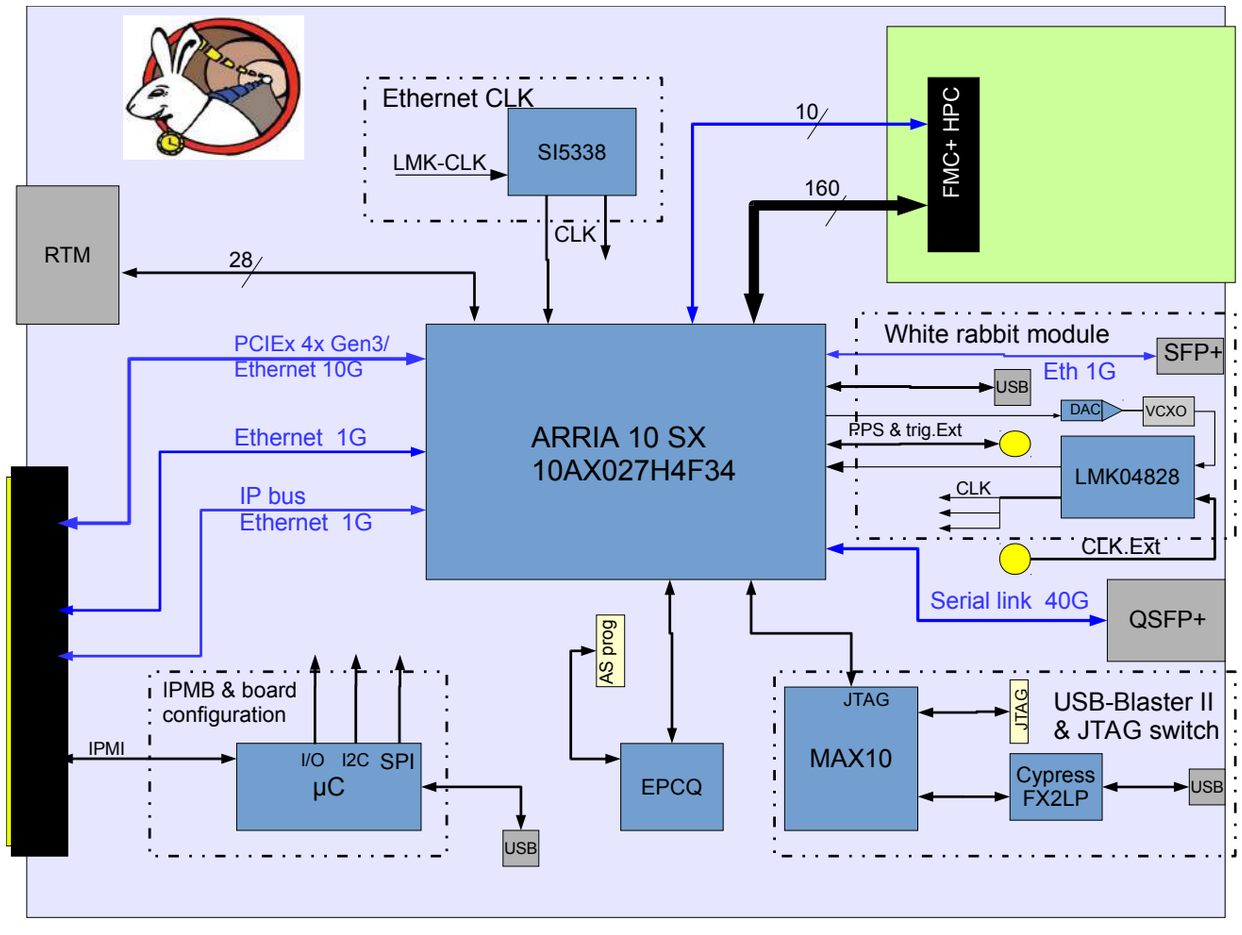
- WR supervision at LAC laboratory
- Monitoring at user equipment level
  - Fibers time propagation delays
  - 1.4Km of fiber
  - 5 network stratum
  - 10 days of measurement
  - Zen-TP system

IDROGEN board

Low phase noise WR -PTP : IDROGEN board

- High performance WR low jitter
- High performance data acquisition system
- Design & realization by IJCLAB
- Design review by M.Lours from SYRTE
- Firmware by Nancay Observatory (C.Viou)
- Expertise for Clock qualification by SYRTE (PE.Pottie)

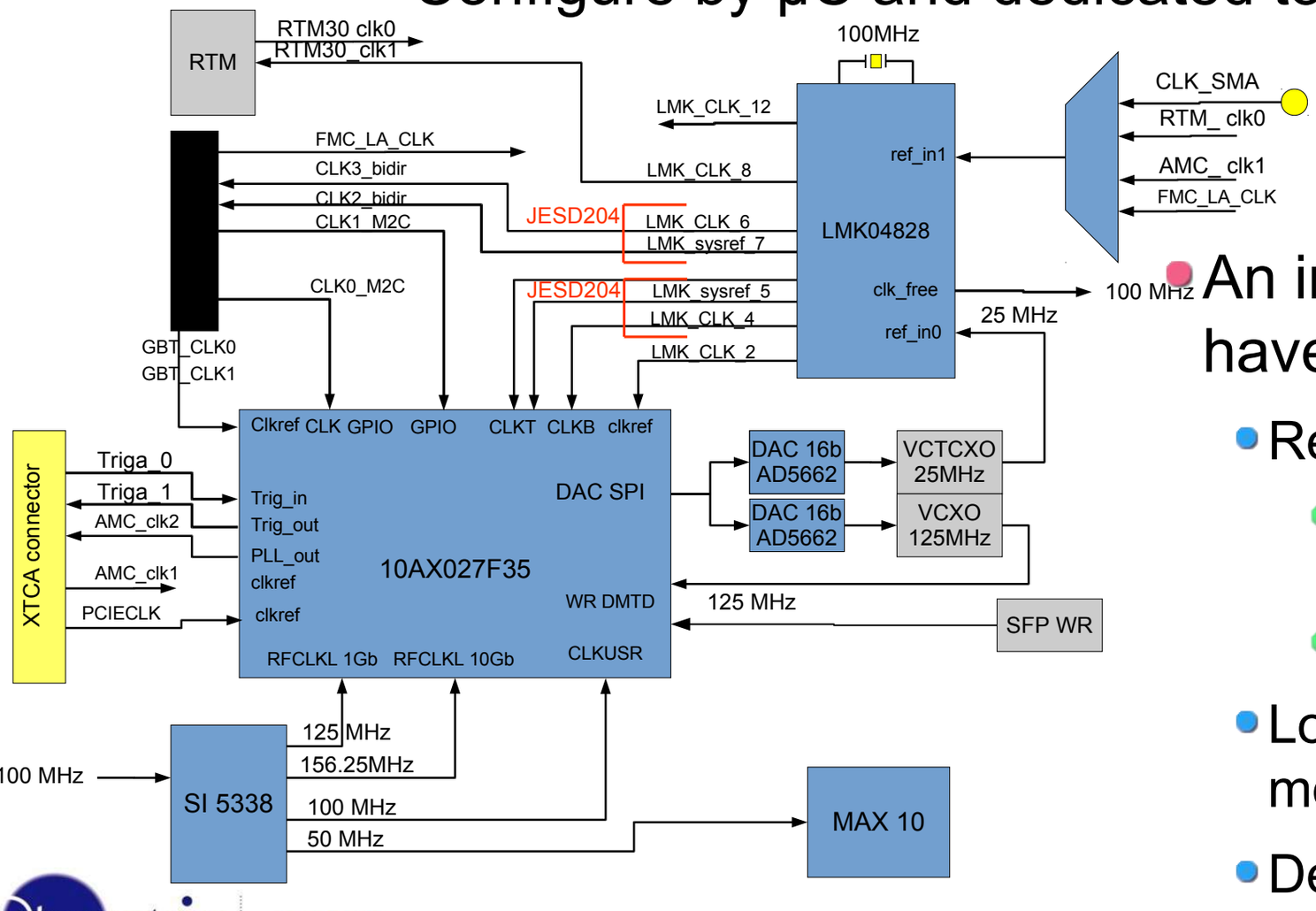
IDROGEN board main features



- MTCA 4.0 standard, double width full-size
- Stand-alone mode
- VITA57.1 (FMC slot)
  - 160 single-ended I/Os (80 LVDS) and/or up to 10 serial transceivers in a 40 x 10 configuration
- Full WhiteRabbit compliant.
- Front panel conectivity
  - WR SFP+
  - QSFP+ 40G, USB
- Backplane connectivity
  - 1Gbe IPbus,PCI 4x Gen3,
  - IPMB, CLK & trigger lane.
  - RTM connector : J30

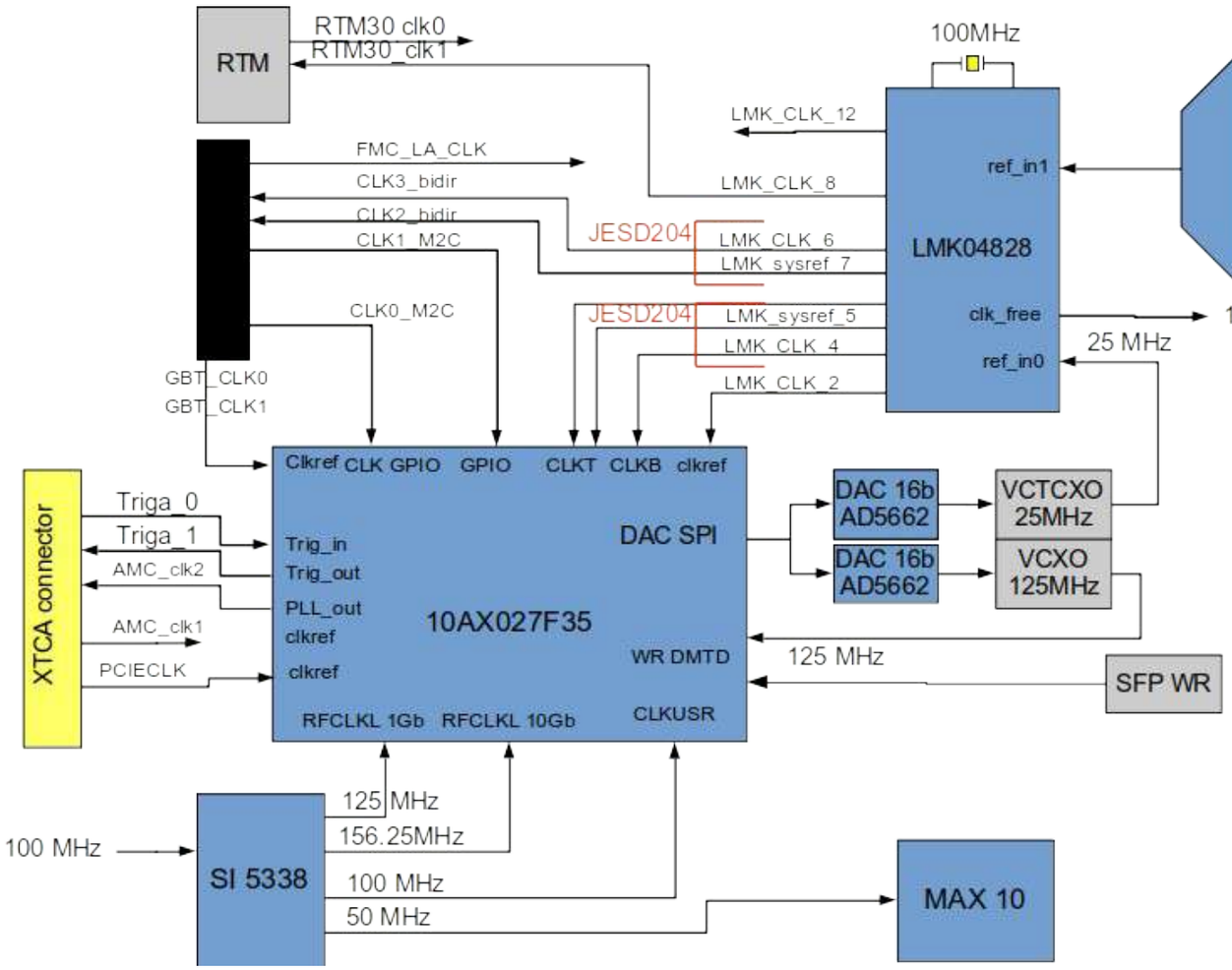
IDROGEN : main features

- 2 Clocks cleaner synthesisers.
  - LM04828 for mains clock ; SI5338 for Ethernet links and services clock
- All clocks on board derive from synthesisers with single sources.
- All clocks routed in differential.
- Two dedicated clocks JESD204 compliant
- Configure by µC and dedicated tools for configuration.



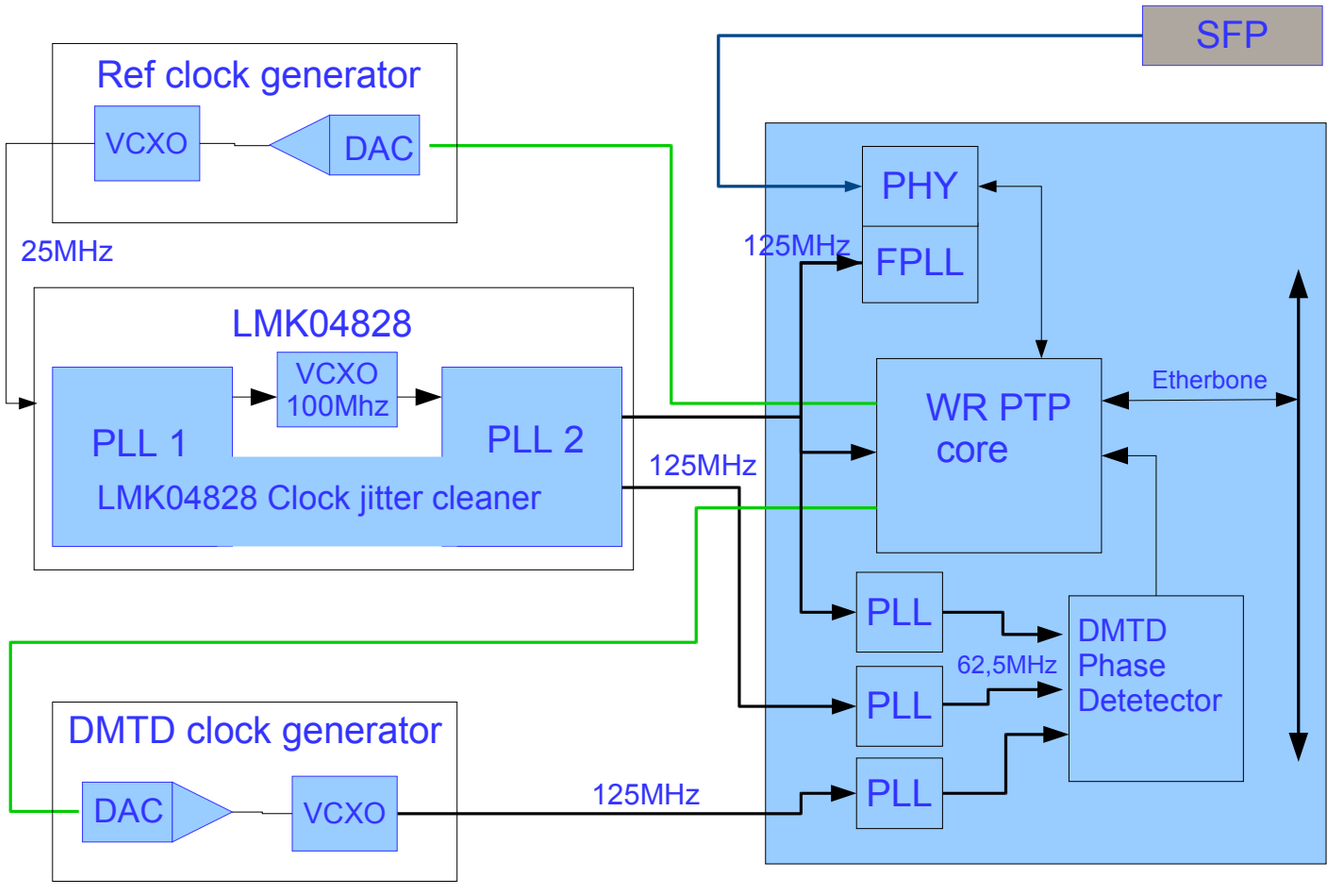
- An improprement of the CERN design have been done :
  - Replacement of the PLL by a LMK04828
    - Ultra low noise clock jitter cleaner with double PLL
    - 90fs RMS jitter
  - Low noise VCXO and ref clock modification
  - Dedicated power supply
  - Rooting and stakup improvment

IDROGEN : Clock tree



- LMK4828 clock in :
  - White-Rabbit module.
  - SMA connector.
  - RMT30 connector : CLK0.
  - FMC connector : LA_CLK.
  - AMC connector : TCLKB.
- LMK4828 clock out :
  - FMC connector JESD204 compliant : Clk2_bidir, Clk3_bidir .
  - RTM : CLK1
  - FPGA : CLKREF, clk.
  - AMC_CLK2
- FPGA receives also direct clocks from different sources :
  - FMC connector
  - AMC connector
  - RTM connector

IDROGEN : White Rabbit implementation



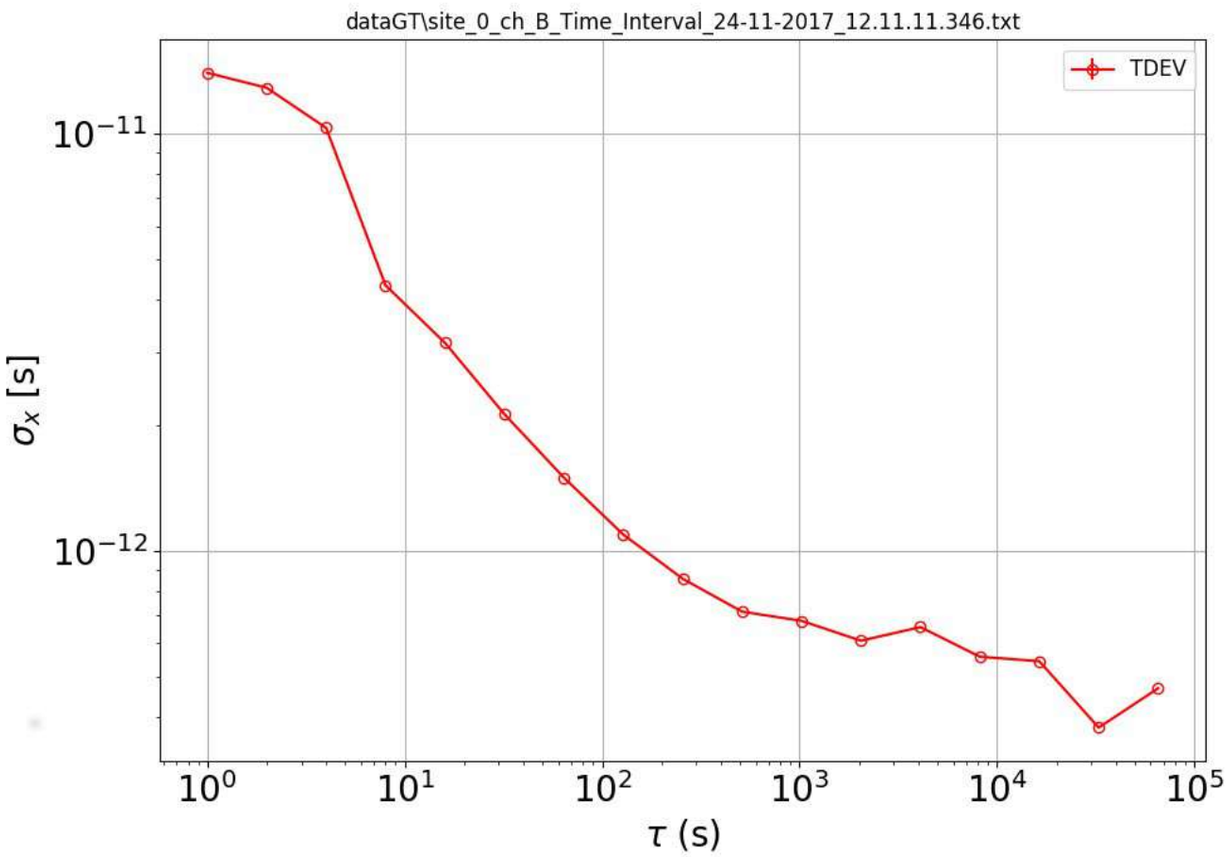
The WhiteRabbit IDROGEN hardware is based on CERN open hardware with Enhancements

- Based on LMK4828 synthetiser
  - Ultra low noise clock jitter Cleaner with Dual Loop PLL
  - 90fs RMS jitter
- DDMTD internal of FPGA (placement with constraint)
- Two generated local clocks :
  - DDMTD source (comparison between WR master clock from SFP)
  - PLL source with phase adjustment
- **IDROGEN Enhancements**
  - PLL selection
  - VCXO Frequency
  - Input frequency for DDMTD
  - Tx/Rx routing equalisation

IDROGEN : Firmwares

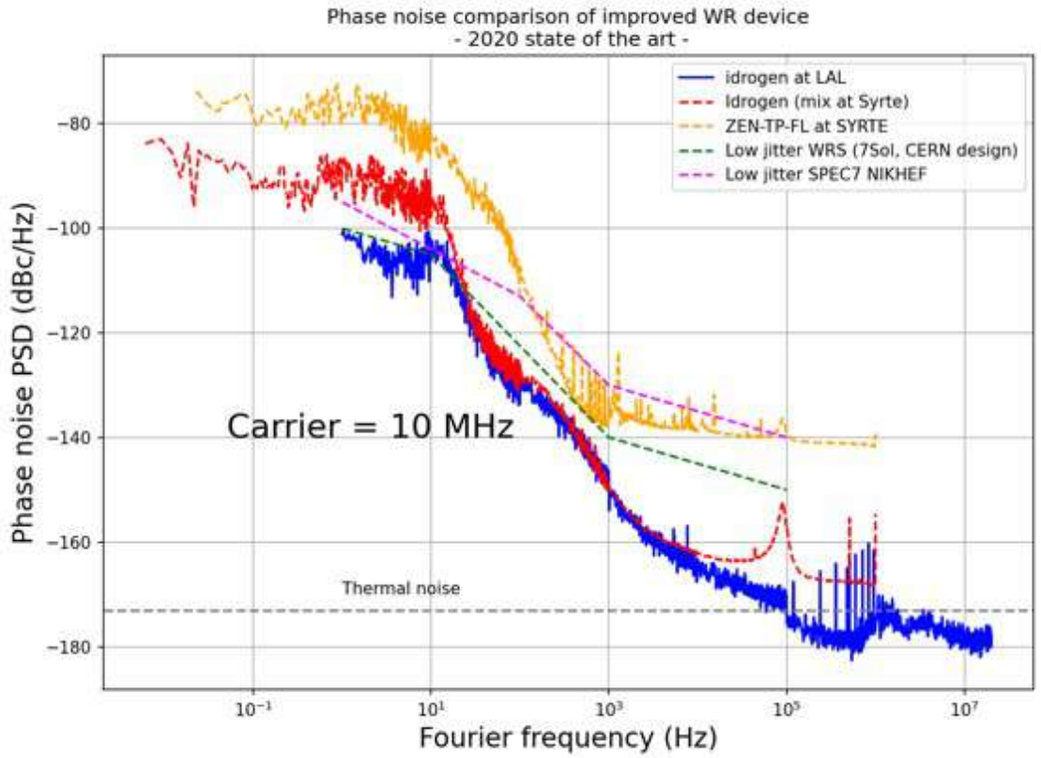
- WhiteRabbit
  - Development of CERN & GSI
  - Adaptation for ARRIA 10
- IpBus 1G & 10G
  - Development of LPSC laboratory
  - Adaptation for ARRIA 10
- Streamer UDP 1G/10G
  - IJCLAB development
- PCIexpress v1
  - Based on INTEL-FPGA
- PCIexpress v2
  - Based on ALICE development
  - High and continuous data rate acquisition
- GBT protocole
  - Based on LHCb for PCIE40 development
- JESD 204B for high speed ADC
  - Basde on INTEL-FPGA IP
- Parallel 64 data acquisition
  - For 2 ADC 125MBPS 16bits
- IpBus on WR link
  - One optical link : timing, synchronisation, configuration, data readout
  - IJCLAB development

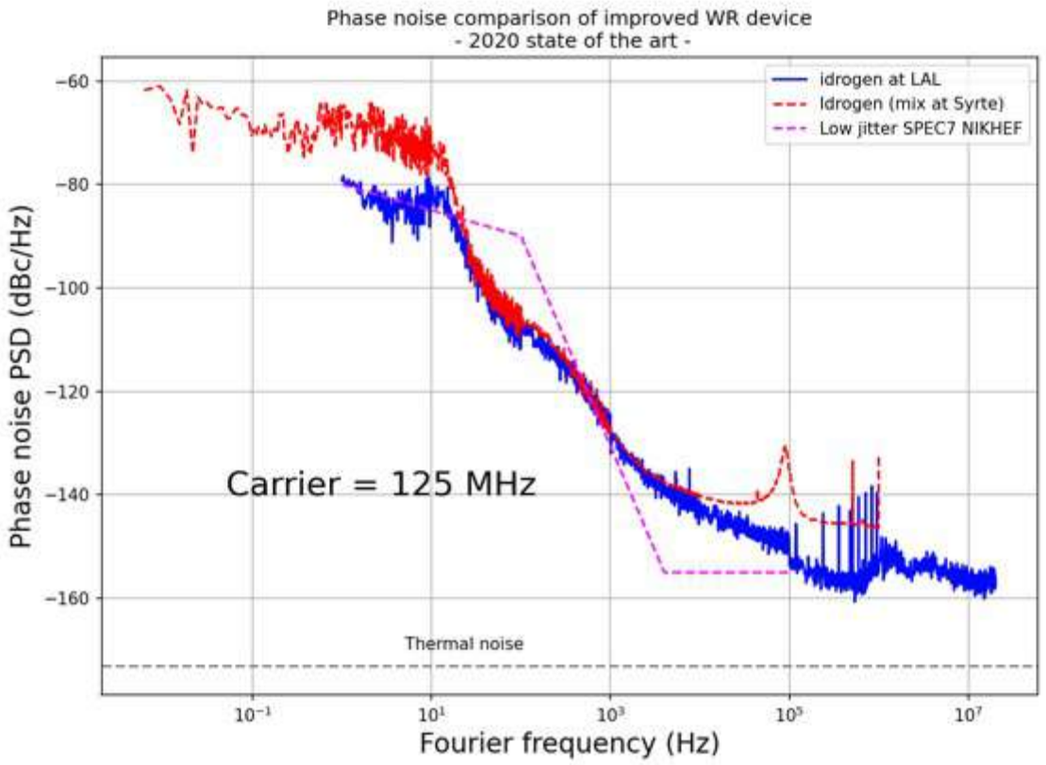
NEBULA performance



- IDROGEN version -1
  - 400fs after 1000s
  - Same design as IDROGEN
  - IDROGEN system qualificationTest
    - With SYRTE test setup

IDROGEN performance

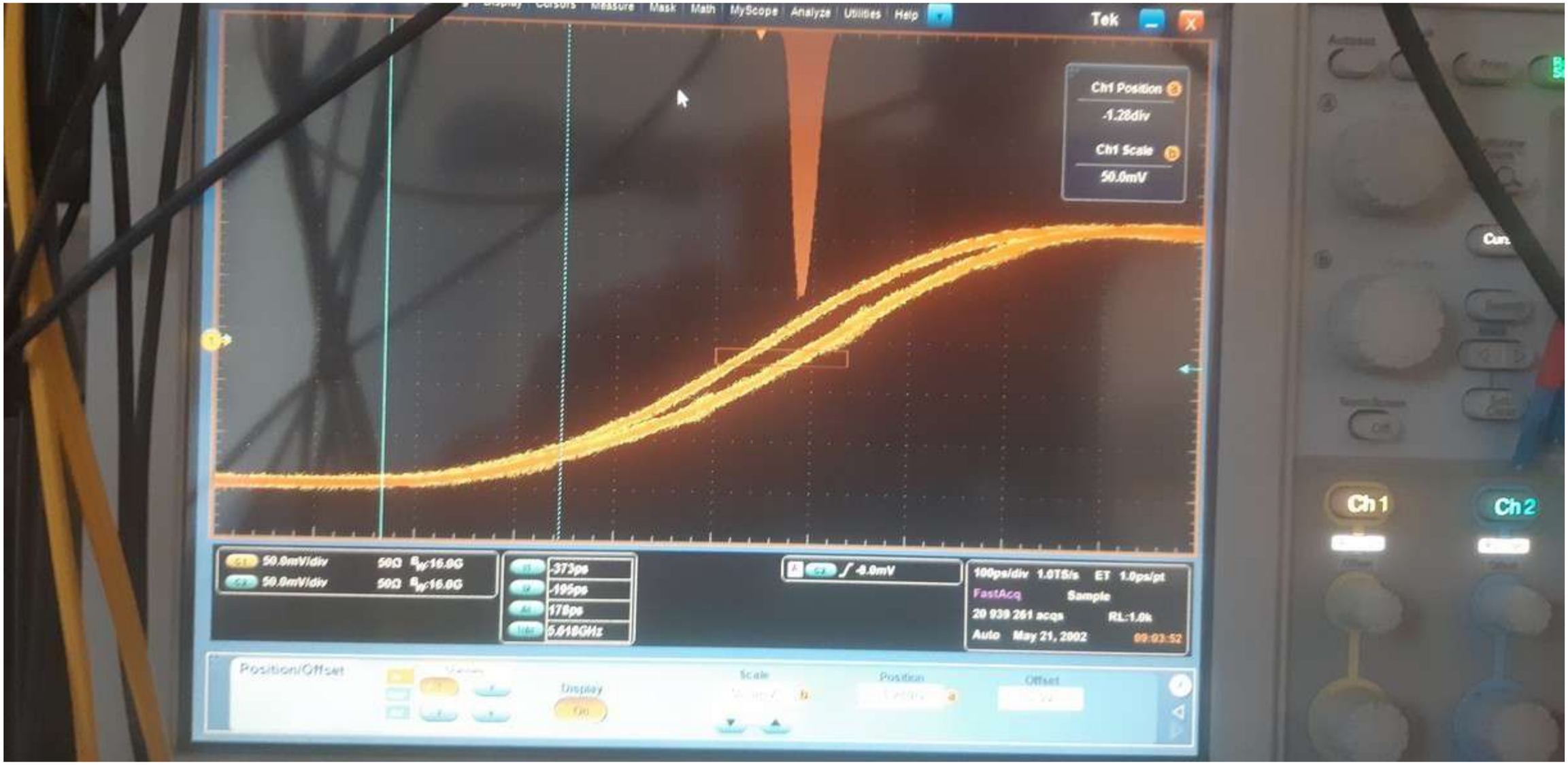




- Transfer from one WR switch to two IDROGEN boards with a short link (few meters)
- For the test we measure the phase difference between 2 nodes (IDROGEN board)
  - Best result, one order of magnitude than the « challenger »
  - Clock phase jitter
  - PPS time precision 1ps RMS

Pulse Per Second : IDROGEN

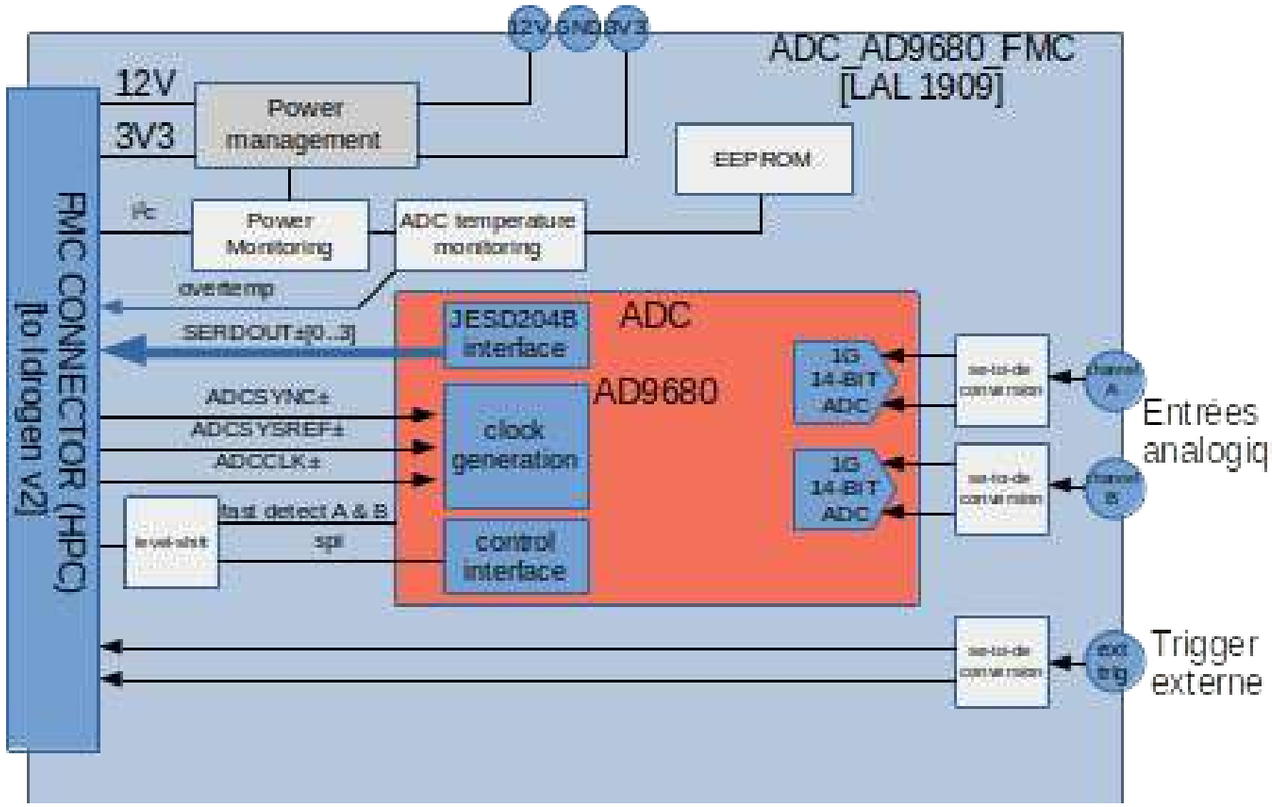
- PPS 2 IDROGEN board
- 25m & 125m of optic fiber
- ~50ps of dispersion of the PPS with calibration



Systèmes de Référence Temps-Espace

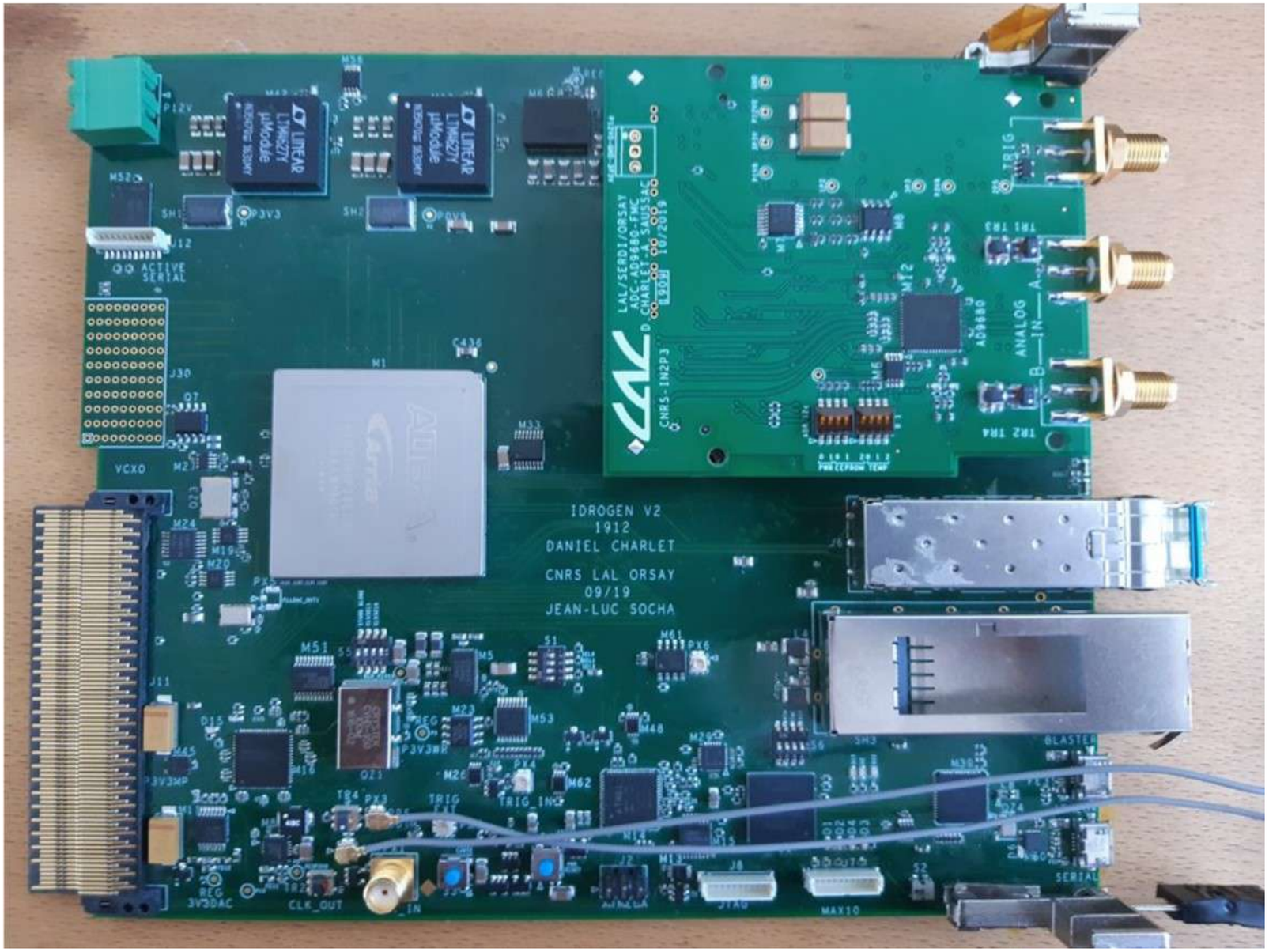
Mezzanine for IDROGEN

Mezzanine FMC ADC 1GSPS



- The motivation of the development of a new mezzanine instead of an off-the-shelf ADC mezzanine :
  - includes : its own PLL.
  - ADC clock source : External clock
- Mezzanine main features :
  - VITA57.1 (FMC)
  - ADC 9680
  - 2 channels
  - 14 bits
  - 1 GSPS
  - JESD204
  - 2GHz analog bandwidth
  - External trigger in

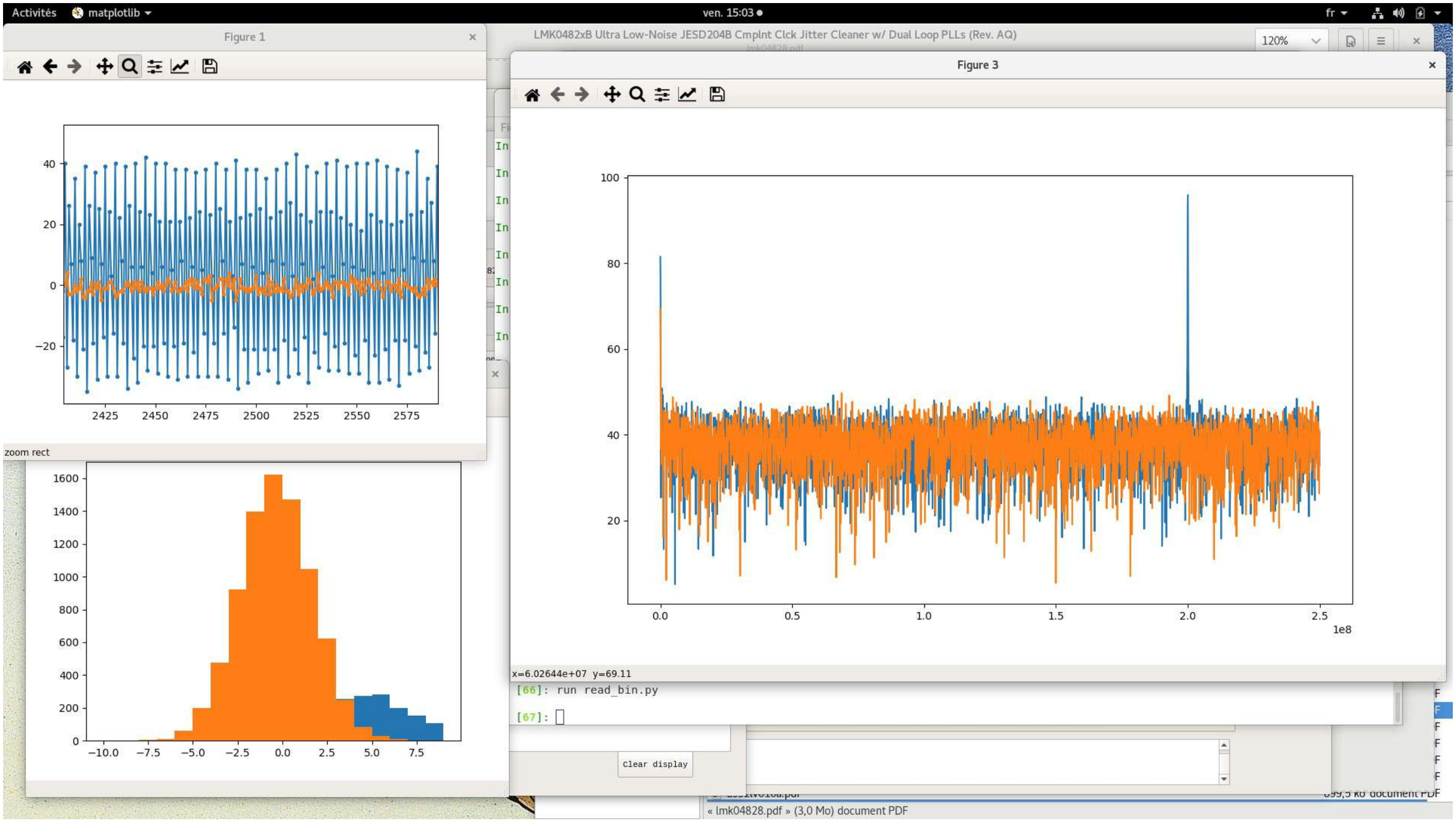
IDROGEN + mezzanine FMC ADC 1GSPS



- Bandwidth 500 MHz to 1.5GHz
- Synchro & timing by WR
- Data transfer 2x 10G Ethernet
- Configuration by IPBus 10G

Systèmes de Référence Temps-Espace

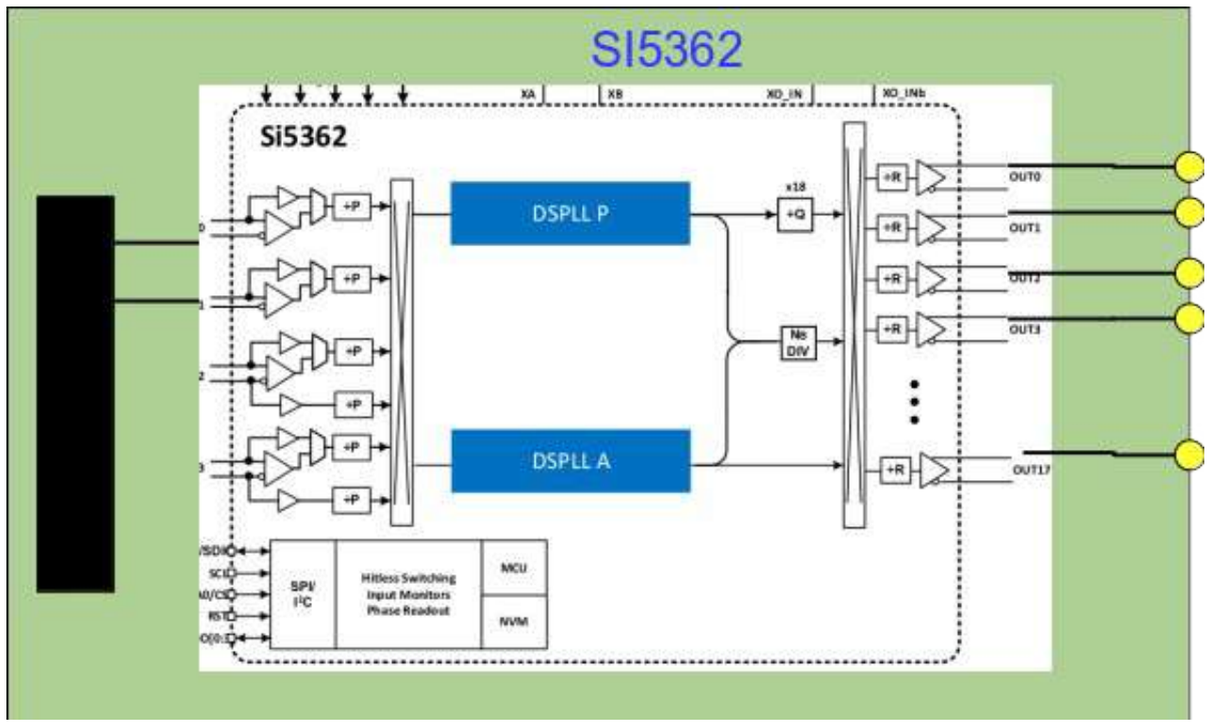
IDROGEN + mezzanine FMC ADC 1GSPS



- Signal at 1.8GHz , 3rd Nyquist band

Systèmes de Référence Temps-Espace

High stability frequency distribution



- Master oscillator distribution
- Implementation of a synthesizer on mezzanine FMC : SI5362
  - Phase jitter 55/100 fs
  - Generation of any frequency :
  - 8KHz < F > 2.75GHz
- Collaboration with accelerator department
- RF filter outside
- Available end 2023

Conclusion

- The White Rabbit is a very powerful protocol
- A majority of new physics experiences will use the WR protocol : CERN detector & accelerator, KEK, Hyper Kamiokande, Enstein telescope...
- A lot of physics experience will be upgrade using WR : CERN experiences, ...
- BUT To go below the ns it’s mandatory to began expert.
- The more precision increases the more experience is required
-